



	17.09 (Friday)	18.09 (Saturday)	19.09 (Sunday)	20.09 (Monday)		
9:00	Registration	Three Plenary Talks (30 min each)	Three Plenary Talks (30 min each)	Three Plenary Talks (30 min each)		
9:30						
10:00						
10:30						
11:00						
11:30					Coffee Break/Posters	
12:00					Regular Papers Session (Room A) (15 min each)	Regular Papers Session (Room A) (15 min each)
12:30	Regular Papers Session (Room A) (15 min each)	Regular Papers Session (Room A) (15 min each)	Regular Papers Session (Room A) (15 min each)			
13:00	Regular Papers Session (Room A) (15 min each)	Regular Papers Session (Room A) (15 min each)	Regular Papers Session (Room A) (15 min each)			
13:30	Regular Papers Session (Room A) (15 min each)	Regular Papers Session (Room A) (15 min each)	Regular Papers Session (Room A) (15 min each)			
14:00	Lunch (each day, 13:30–15:00)					
14:30	Lunch (each day, 13:30–15:00)					
15:00	Opening Session	Social Event: Boat Trip by St.Petersburg Channels				
15:30	Three Plenary Talks (30 min each)					
16:00	Coffee Break					
16:30					Regular Papers Session (Room A) (15 min each)	
17:00	Regular Papers Session (Room A) (15 min each)	Social Event: Great Peterhof Palace				
17:30	Regular Papers Session (Room A) (15 min each)					
18:00	Regular Papers Session (Room A) (15 min each)					
18:30	Regular Papers Session (Room A) (15 min each)					
19:00	Free time	Free Time				
19:30	Free time					
20:00	Welcome Reception					
20:30					Free Time	
21:00		Gala Dinner				
21:30						



FROM THE ORGANIZING COMMITTEE

We have great pleasure to invite you to IEEE EAST-WEST DESIGN & TEST SYMPOSIUM – EWDTS'10!

The purpose of the symposium is to coordinate and exchange experiences between leading scientific organizations and experts of the Eastern and Western Europe, as well as of the USA in the field of digital systems design and test.

From the one side, an overview of the state-of-the-art and of the most important progress trends of the industrial design and test will be presented by leading researchers and practitioners.

On the other side, an overview of recent achievements obtained by the scientists and technologists will be presented by the researchers and practitioners from countries in the region.

We are happy that EWDTS is becoming a world-renown event, as we have seen the interest of Eastern and Western scientists in mutual collaboration. As a result of this collaboration we can see the penetration of new technologies in the Eastern Europe market and educational system.

We would like to thank: Yervant Zorian, Raimund Ubar, Dmitry Bykov, Vladimir M. Kutuzov, Michael Yu. Shestopalov, S. Shaposhnikov, A. Korotkov, Zainalabedin Navabi, Viktor Djigan for taking an active role in organizing the conference technical program and finances, in international activity in the field of higher education in Ukraine, and in support the preparation and operation of the symposium. The greatest appreciation to the official EWDTS'10 technical sponsor, the IEEE Computer Society Test Technology Technical Council – TTTC, and financial supporters, St. Petersburg State Electrotechnical University «LETI», Virage Logic, Aldec, Synopsys, Kaspersky Lab, DataArt Lab, Tallinn Technical University, JTAG Technologies, and Donetsk Academy of Road Transport. We especially thank the Rectors: Vladimir Kutuzov — Saint Petersburg Electrotechnical University "LETI" and Mikhail Bondarenko – Kharkov National University of Radio Electronics for overall support and active personal participation in preparation and holding of the symposium.

We welcome all the participants of the symposium and wish you successful discussions and a pleasant stay in St. Petersburg!



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The Technical Sponsor of the 8th IEEE East-West Design & Test Symposium is IEEE COMPUTER SOCIETY'S Test Technology Technical Council (TTTC).



The Test Technology Technical Council is a volunteer professional organization sponsored by IEEE Computer Society. Its mission is to contribute to members' professional development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the-art in test technology.

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IEEE DESIGN & TEST OF COMPUTERS



IEEE D&T is a bimonthly magazine published by the IEEE Computer Society in cooperation with the IEEE Circuits and Systems Society specifically for design and test engineers, and researchers. D&T features peer-reviewed original work describing methods and practices used to design and test electronic product hardware and supportive software. Articles explore current practices and experience in: System Level Design and Test; Embedded Test Technology; Low Power Design; Reconfigurable



Systems; Board and System Test; Analog and Mixed Signal Design and Test; System-on-Chip Design and IP Reuse; Embedded Systems and Software; Design and Verification.

PAPER SUBMISSION: Authors should use Manuscript Central (<https://mc.manuscriptcentral.com/cs-ieee>) to upload their submissions. The first-time user must create a new account. The site provides detailed instructions on usage. Each submitted paper undergoes at least three technical reviews. All submissions must be original, previously unpublished work.

Scientific and Technical Journal

RADIOELECTRONICS AND INFORMATICS

A Journal serving electronic and test professionals in concurrence with the Test Technology Technical Council (TTTC) of the IEEE Computer Society. The main target is to exchange experiences between the scientists and technologies of the Eastern and Western Europe, as well as North America and other parts of the world, in the field of Computer Engineering (Design automation and test of electronic systems), Computer Science, Radiotechnics (RF Design), Microelectronics, HDTV, and Telecommunications.

The main features of R&I Journal are: 1) English language. 2) IEEE CS (like IEEE Transactions on ...) format of camera-ready. 3) Reviewed by 3 independent and blind reviewers. 4) Covered by IEEE index and included into IEEE library. 5) Publisher – Kharkov National University of Radio Electronics. 6) <http://www.ewdtest.com/ri>

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GENERAL INFORMATION AND INQUIRIES

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BANKING

Generally, everywhere in Russia you pay in Russian rubles (RUB). The currency units are: ruble and copeck: 1 RUB = 100 copecks. The Russian RUB is a fully convertible currency internally in Russia.



Foreign currency exchange facilities are available at major airports, railway stations, at large hotels, as well as in many private offices, called "Currency exchange". Credit cards can be used in such places as banks and branch banks. Approximate currency exchange rate: 1 USD = 30,86 RUB (100 USD = 3086 RUB), 1 EURO = 39,01 RUB (100 EURO = 3901 RUB)

CREDIT CARDS: Visa Card and Master Card are the most common cards. However, other cards are also accepted.

PROGRAM OF THE SYMPOSIUM

The program of the EWDTs'10 symposium will consist of presentations of contributed keynotes, invited and regular papers. The language of the conference is English, neither translation nor interpretation will be provided.

The presentation time for regular papers is 15 minutes and keynotes/invited talks is 30 minutes.

Social events, covered by regular registration fee, are Welcome Reception and Gala Dinner, Excursion to the Great Peterhof Palace and Park, Trip by St. Petersburg Channels.

WEATHER

September in St. Petersburg is rather cold. The temperature can be typically 5-10 degrees Centigrade during days and rain. During nights, the temperature can drop to 0-5 degrees Centigrade.

GENERAL INFORMATION

Total number of authors: 216.

Number of accepted papers: 111.

Number of participating countries: 34 (Armenia, Azerbaijan, Bangladesh, Belarus, Brazil, Côte d'Ivoire, Croatia, Egypt, Estonia, Finland, France, Germany, India, Iran, Israel, Italy, Japan, Jordan, Luxembourg, Mexico, Nigeria, Norway, Poland, Colombia, Canada, Romania, Russia, Saudi Arabia, Singapore, Syria, Sweden, UK, Ukraine, USA).

Number of keynotes is 4 and number of invited talk is 12.

Number of Universities and Companies is 82.

Number of cities is 57.



SAINT PETERSBURG ELECTROTECHNICAL UNIVERSITY "LETI" (ETU)



Saint Petersburg Electrotechnical University "LETI" (ETU) has an outstanding reputation as a higher education institution with strong traditions. ETU is considered as one of the world largest education and research centres in Radio Engineering, Electrical Engineering, Electronics and Computer Science.

ETU has more than 1000 highly-qualified staff (a 70% Ph.D. rate), 30 of them have Russian and international prizes. Over 30 academicians and members of the Russian Academy of Science worked at ETU.

The Nobel Prize Winner in physics Zhores Alferov is the head of the department of optoelectronics.

ETU was Alma Mater for over 70,000 students and over 3,000 international students.

Over 8,000 students and 400 postgraduates attend 82,000 sq.m ETU campus located just in the downtown of Saint Petersburg.



Annually over 2,000 prospective students attend pre-university courses. ETU has state-of-the-art facilities and equipment. Research in Microelectronics, Solid State Physics, Parallel Computer Networks is carried out using unique technological and computer equipment.

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KHARKOV NATIONAL UNIVERSITY OF RADIO ELECTRONICS



Kharkov National University of Radioelectronics was founded 80 years ago. It was the best University in USSR in 70th – 90th in the field of radio electronics. Today the University is the leader among all technical universities of Ukraine. Total number of students is more than 11000. The number of PhD and Doctoral students is more than 250. There are 650 teachers working for University. Among them there are 150 professors and 450 PhD. Every year the University graduates more than 1,832 bachelors, 1,537 specialists, 184 masters. Graduate students work in USA, Germany, England, Finland, France, Poland, Russia, and Bulgaria.



The University has close contacts with more than 150 universities from the world including: Germany, USA, UK, France, Japan, China, Bulgaria, Finland, Netherlands, Greece, Russia, Byelorussia, Czech Republic, Mexico, Serbia.

The University consists of 7 faculties. The faculty of Computer Engineering and Control is one of the best among the technical universities, which have similar specialties. During last ten years it has been taking an active part in scientific activities of state in the field of computer systems and networks design and application. The faculty consists of 4 departments, 1500 students (300 foreign students from 31 countries).

SYMPOSIUM PROGRAM

First Day: September 17th, 2010 (Friday)	
09:00—13:00	Registration
13:30—15:00	Lunch
15:00—15:10	Opening Session Vladimir M. Kutuzov — <i>rector of Saint Petersburg Electrotechnical University "LETI", Russia</i> Yervant Zorian — <i>EWDTS General Chair, and Vice President, Virage Logic, USA</i> Michail Yu. Shestopalov — <i>Vice Rector of Saint Petersburg Electrotechnical University "LETI", Russia</i> Vladimir Hahanov — <i>EWDTS General Chair, and Kharkiv National University of Radio Electronics, Ukraine</i>
15:10—17:30	Plenary Session A Moderator: Michail Shestopalov — <i>Saint Petersburg Electrotechnical University "LETI", Russia</i>
15:10—15:30	Keynote Address: The Emerging Adaptive Test Methodology Adit Singh — <i>Auburn University, USA</i>
15:30—16:00	Invited Talks: Secure Communication Protocol for Wireless Sensor Networks Cecilia Metra — <i>University of Bologna, Italy</i>



First Day: September 17th, 2010 (Friday)

16:00—16:30 **An Update on The Semiconductor Industry Landscape: Disaster Averted**

Rich Goldman — *Synopsys, Armenia*

16:30—17:00 **Cluster Test Alternatives Using Boundary-Scan Technology**

Alexey Ivanov and Mick Austin — *JTAG Technologies, Finland*

17:00—17:30 **IT Security Development by Kaspersky Academy**

Svetlana Efimova — *Head of educational programs, Kaspersky Academy, Russia*

Irina Selezneva — *Education Programs Coordinator, Kaspersky Academy, Russia*

17:30—18:00 **Coffee Break**

18:00—20:15 **Session 1-A: CAD Tools in Design & Test (1)**

Moderator: Alexander Drozd — *Odessa National Polytechnic University, Ukraine*

A Technique of Optimal Built-In Self-Test Circuitries Generation

Natalia V. Chebykina, Sergey G. Mosin — *Vladimir State University, Russia*

Stable Current and Voltage Generation under Process Variation

Vazgen Melikyan, Sh. Karapetyan, D. Mirzoyan, E. Babayan — *Synopsys Armenia CJSC, Armenia*

On Selection of State Variables for Delay Test of Identical Functional Units

Sinsinwar G., Choudhary R. R. — *Govt. Engineering College, India*

Aditi Kajala — *Mody Institute of Technology and Science, India*

Virendra Singh, Jaynarayan Tudu — *Indian Institute of Science, India*



First Day: September 17th, 2010 (Friday)

A Process Variation Detection Method

Vazgen Melikyan, Davit Mirzoyan, Gor Petrosyan
— *Synopsys Armenia CJSC, Armenia*

Architecture of Queued-Free Crossbar for On-Chip Networks

Gor Petrosyan, Sargis Abovyan, Tigran Harutyunyan – *Synopsys Armenia CJSC, Armenia*

Test Program Generation for Simultaneous Testing of Multiple Identical Functional Units in Super-scalar Architecture

Sinsinwar G., Choudhary R. R – *Govt. Engineering College, India*

Aditi Kajala — *Mody Institute of Technology and Science, India*

Virendra Singh – *Indian Institute of Science, India*

Fault Grading using Instruction-Execution Graph

K. R. Vinutha, Virendra Singh — *Indian Institute of Science, India*

Anzhela Matrosova — *Tomsk State University, Russian Federation*

M. S. Gaur — *Malaviya National Institute of Technology, Jaipur, India*

The Crosstalk Faults Test Generation

Yu. A. Skobtsov, Iyad K.M. Nasser — *Donetsk National Technical University, Ukraine,*

V. Yu. Skobtsov — *National Academy of Sciences of Ukraine, Ukraine*

Multi-level Thermal Design of Electronic Components: from Submicron Devices and ICs to Systems on a Board

Petrosyants K.O., Kozyanko P.A., Kharitonov I.A., Rjabov N.I. — *Moscow State Institute of Electronics and Mathematics, Russia*

Internet Applications Testing Automation Through Probabilistic-Network Programming

Bykau A. A., Piletsky I. I — *EPAM Systems, IBA*



First Day: September 17th, 2010 (Friday)

18:00—20:15 **Session 1-B: Analysis and Optimization**
Moderator: Sergey Mosin — *Russia*

Test Minimization Technique for Multiple Stuck-at Faults of Combinational Circuit

V. Andreeva — *Tomsk State University, Russia*

Modeling On-Chip Variations in Digital Circuits Using Statistical Timing Analysis

Gor Petrosyan, Sargis Abovyan, Tigran Harutyunyan — *Synopsys Armenia CJSC, Armenia*

Hardware Reduction for FSM – Based Control Units Using PAL Technology

A. Barkalov, L. Titarenko, S. Chmielewski — *Institute of Computer Engineering and Electronics, Poland*

Matrix Implementation of Moore FSM with Encoding of Collections of Microoperations

A. Barkalov, L. Titarenko, O. Hebda — *Institute of Computer Engineering and Electronics, Poland*
K. Soldatov — *Donetsk National Technical University, Ukraine*

Dynamic Characteristics of Different System Design Strategies

A. M. Zemliak — *Puebla Autonomous University, Mexico, Kiev National Technical University of Ukraine, Ukraine*
M.A. Torres, F. Reyes, S. Vergara — *Puebla Autonomous University, Mexico*
T.M. Markina — *Kiev National Technical University of Ukraine, Ukraine*

Methodology of Algorithms Synthesis of Storage Devices Test Diagnosing

Mudar Almadi, Diaa Moamar, Vladimir Ryabtsev — *Cherkassy Branch of the European University, Ukraine*



First Day: September 17th, 2010 (Friday)

Metastability Testing at FPGA Circuit Design using Propagation Time Characterization

Branka Medved Rogina, Peter Škoda,
Karolj Skala, Ivan Michieli — *Ruđer Bošković
Institute, Croatia*

Maja Vlah, Siniša Marijan — *Electrical
Engineering Institute, Croatia*

GA-based and Design by Contract Approach to Test Generation for EFSMs

Andrey Zakonov, Oleg Stepanov, Anatoly Shalyto
— *St. Petersburg State University of Information
Technologies, Mechanics and Optics, Saint-
Petersburg, Russia*

Models of Synchronous Hardware Designs Based on FSM at Different Abstraction Levels: Application to Functional Verification

Mikhail Chupilko — *Institute for System
Programming of the Russian Academy of
Sciences*

CTestBench: A Lightweight C-Based Tool for Specification and Functional Verification of Hardware Designs

Kamkin A. — *Institute for System Programming of
the Russian Academy of Sciences*

20:15—20:30 **Free Time**

20:30—22:00 **Welcome Reception**

Second Day: September 18th, 2010 (Saturday)

09:00—11:00 **Plenary Session B**

Moderator: Liviu Miclea — *Romania*

09:00—09:30 **Keynote Address**

Impact of New Technologies on Test & Yield

Yervant Zorian — *Virage Logic, USA*



Second Day: September 18th, 2010 (Saturday)

09:30—10:00	Invited Talks: Cyber Space and Brain-like Computing Vladimir Hahanov, Eugenia Litvinova, Svetlana Chumachenko — <i>Kharkov National University of Radioelectronics, Kharkov, Ukraine</i> Wajeb Gharibi — <i>Jazan University, Kingdom of Saudi Arabia</i>
10:00—10:30	Fault-Detection Capability Analysis of a Hardware-Scheduler IP-Core In Electromagnetic Interference Environment Fabian Vargas — <i>Catholic University, Brazil</i>
10:30—11:00	Power Aware Design Automation of Transistor Networks Ricardo Reis — <i>UFRGS, Brazil</i>
11:00—11:30	Coffee Break
11:30—13:30	Session 2-A: CAD Tools for Design & Test (2) Moderator: Vyacheslav Kharchenko — <i>Ukraine</i>
	Multi-level Methodology for CMOS SOI/SOS MOSFET Parameterization for IC Radiation Hardness Simulation with SPICE I. A. Kharitonov,— <i>Moscow State Institute of Electronics and Mathematics (Technical University), Russia</i>
	Minimal Algorithms for Testing Content-Addressable Memories H. Grigoryan, G. Harutynian, S. Shoukourian, V. Vardanian, Y. Zorian, <i>Virage Logic, Armenia</i>
	Component-Based Safety-Oriented On-Line Testing of Digital Systems A. Drozd, V. Kharchenko, A. Siora, V. Sklyar — <i>Odessa National Polytechnic University, Ukraine</i>
	Virtual Tester Development Using HDL/PLI Arezoo Kamran, Nastaran Nemati, Somayeh Sadeghi Kohan, Zainalabedin Navabi — <i>U. of Tehran, Iran</i>



Second Day: September 18th, 2010 (Saturday)

Virtual Web-Laboratory on Testware for Digital Circuits

Victor Zviagin— *National Research University ITMO (IT, Mechanics and Optics, Russia)*

Self-Testing of Microcontrollers in the Field

Janusz Sosnowski — *Warsaw University of Technology, Poland*

Boundary Scan: Reduced Pin Count Test Solution

Surendra Batukdeo — *Institute of Technical Education, Singapore*

An Efficient March Test for Detection of All Two-Operation Dynamic Faults from Subclass S_{av}

Sargis Abovyan, Tigran Harutyunyan, Gor Petrosyan — *Synopsys Armenia CJSC, Armenia*

Component Architecture with Runtime Type Definition

Gringkrug Efim Mikhaylovich, Shakurov Amir Rafailovich — *Higher School of Economics, Russia*

Merit Based Directed Random Test Generation (MDRTG) Scheme for Combinational Circuits

Arezoo Kamran, Mohammad Saeed Jahangiry and Zainalabedin Navabi — *University of Tehran, Iran*

Verification of FPGA Electronic Designs for Nuclear Reactor Trip Systems: Test- and Invariant-Based Methods

V. Dovgopolyi, V. Golovir – *Research and Production Corporation "Radyi"*

A. Andrashov, V. Kharchenko, V. Sklyar, L. Reva — *National Aerospace University "KhAI", Ukraine*



Second Day: September 18th, 2010 (Saturday)

11:30—13:30 **Session 2-B: High-level Synthesis. SL-Modeling, Simulation and Test Generation**
Moderator: Angella Matrosova

Exploring Modeling and Testing of NAND Flash memories

Michele FABIANO, Roberto PIAZZA, Paolo PRINETTO — *Politecnico di Torino, Italy*

Communication Interface Synthesis from TLM 2.0 to RTL

Nadereh Hatami, Marco Indaco, Paolo Prinetto, Gabrielle Tiotto — *Politecnico di Torino, Italy*

Testing Beyond the SoCs in a Lego Style

A. Tsertov, A. Jutman. S. Devadze — *Tallinn University of Technology, Estonia*

Microprogram control unit with code sharing and extended microinstruction format

Alexander Barkalov, Larysa Titarenko, Jacek Bieganski — *University of Zielona Góra, Poland*

An Algorithm of Timing Recovery for Modem with M-ary Alphabets APK-Signals

Victor V. Panteleev — *TELNET, Ltd., Ukraine*

Engineering-Maintenance Methods of the Calculation xDSL-lines

Victor V. Panteleev, Alexander I. Vakaruk — *TELNET, Ltd., Ukraine*

ESL Design Methodology for Architecture Exploration

Fatemeh Javaheri, Zainalabedin Navabi — *University of Tehran, Iran*

Virtual Tester Development Using HDL/PLI

Arezoo Kamran, Nastaran Nemati, Somayeh Sadeghi Kohan and Zainalabedin Navabi — *University of Tehran, Iran*



Second Day: September 18th, 2010 (Saturday)

The Simulation of PNP-Transistor as an Element of High-Voltage Integrated Circuits by Various Parameters of Epitaxial Film

Dudar N.L. — *Openly Join-Stock Company «Integral», Minsk, Republic of Belarus*

Borzdov V.M. — *Belarusian State University, Minsk, Republic of Belarus*

RTL IP Abstraction into Optimized Embedded Software

Nicola Bombieri, Diego Forrini, Franco Fummi, Matteo Laurenzi and Sara Vinco — *University of Verona, Italy*

A Method for Automatic Generation of an RTL-Interface from a C++ Description

Obrizan V. — *Kharkov National University of Radioelectronics (KHNURE), Kharkov, Ukraine*

13:30—15:00 **Lunch**

15:00—20:00 **Social Event: Trip by St.Petersburg Channels**

Third Day: September 19th, 2010 (Sunday)

09:00—11:00 **Plenary Session C**
Moderator: Fabian Vargas, Brazil

09:00—09:30 **Keynote Address:**
Sign Language Synthesis Using Hand Motion Acquisition
Paolo Prinetto — *Politecnico di Torino, Italy*

09:30—10:00 **Invited Talks:**
Encryption Algorithms for Structured Systems
Liviu Miclea — *Technical University of Cluj-Napoca, Romania*



Third Day: September 19th, 2010 (Sunday)

10:00—10:30 **Beyond RTL: ESL Design Methodology, Simulation, Synthesis, and Test**
Zainalabedin Navabi — *University of Tehran, Iran*

10:30—11:00 **An Approach for PSL Assertion Coverage Analysis with High-Level Decision Diagrams**
Maksim Jenihhin, Jaan Raik, Raimund Ubar, Tatjana Shchenova — *Tallinn University of Technology, Estonia*

11:00—11:30 **Coffee Break**

11:30—13:30 **Session 3-A: Signal Processing**
Moderator: Victor I. Djigan — *Electronic VLSI Engineering & Embedded Systems R&D Center of Microelectronics, Russia*

Quantization Step Dispersion of Direct Transformation ADC

Stanislav Gritsutenko, Aleksey G. Panyukov — *Omsk State Transport University, Russia*

Performance Investigation of Antenna Arrays by Means of Virtual Instruments

Victor I. Djigan — *Electronic VLSI Engineering & Embedded Systems R&D Center of Microelectronics, Russia*

Quantization Step Dispersion of Direct Transformation ADC

Stanislav S. Gritsutenko, Aleksey G. Panyukov — *Omsk State Transport University, Russia*

The Digital Signal Processing CAD System

Ilya V. Parnevich — *Computer Engineering Department, Vladimir State University, Russia*

Adaptive Array Based on “Multicore” DSP Family and Linearly Constrained Constant Modulus IQRD RLS Algorithm

Irina D. Pletneva — *Telecommunication System*



Third Day: September 19th, 2010 (Sunday)

Department, Moscow State Institute of Electronic Technology, Russia

Victor I. Djigan — *Electronic VLSI Engineering & Embedded Systems R&D Center of Microelectronics, Russia*

Level Quantization Effect on Accuracy of Fast Fourier Transform Algorithm

Gamlet S. Khanyan — *Central Institute of Aviation Motors, Russia*

Blind Carrier Frequency Offset Estimation for QAM Signals Based on Weighted 4th Power of Signal Samples

Alexander B. Sergienko, Alexander V. Petrov — *Department of Theoretical Fundamentals of Radio Engineering, Russia*

Implementation of a New Paradigm in Design of IIR Digital Filters

Vladislav A. Lesnikov, Alexander V. Chastikov, Tatiana V. Naumovich — *Vyatka State University, Russia*

Sergey V. Armishev — *Rondosoft, USA*

FPGA-based Digital Phase Difference Meter

Vdovychenko Y. I. — *Ukraine Central State Designs Bureau "Proton", Ukraine*

Estimated Formation Probability of Meteoric Trails with Mirror Reflection

Helen V. Kharchenko, A.Y. Usikov — *Institute of Radio Physics and Electronics NAS of Ukraine, Ukraine*

Straight Edge Extraction and Localization on noisy Images

V. Volkov, A. Oneshko, D. Oralov — *The Bonch-Bruевич State University of Telecommunications, Russia*

R. Germer — *The Hochschule für Technik und Wirtschaft, Germany*



Third Day: September 19th, 2010 (Sunday)

11:30—13:30 **Session 3-B: Reliability, Fault Tolerance, Testability**

Moderator: Ilya Levin – Israel

High-Density Layout Designing of CMOS VLSI Parameterized Fragments

I. S. Zuev, A. Maximov — *Saint-Petersburg State Electrotechnical University “LETI”, St.-Petersburg, Russia*

PDFs Testing of Combinational Circuits Based on Covering ROBDDs

Matrosova A., Nikolaeva E. — *Tomsk State University, Russia*

Experiments with ABIST Test Methodology Applied to Path Delay Fault Testing

P. Manikandan, Bjørn B. Larsen, Einar J. Aas — *The Norwegian University of Science and Technology, Norway*

A TLM2.0 Assertion Library with Centralized Monitoring Approach

Sheis Abolma'ali— *Semnan University, Iran*
AmirAli Ghofrani, Zahra Najafi Haghi,
Zainalabedin Navabi — *University of Tehran, Iran*

Near Optimal Machine Learning Based Random Test Generation

Niki Shakeri, Nastaran Nemati, Majid Nili
Ahmadabadi, Zainalabedin Navabi — *University of Tehran, Iran*

Configurable Architecture for Memory BIST

Atieh Lotfi, Parisa Kabiri, Zainalabedin Navabi — *University of Tehran, Iran*

Path Delay Faults and ENF

A. Matrosova, V. Lipsky, A. Melnikov — *Tomsk State University, Russia*
Virendra Singh — *Indian Institute of Science, India*



Third Day: September 19th, 2010 (Sunday)

Testable Combinational Circuit Design, Based on ZDD-implementation of ISOP Boolean Function

S. Ostanin, R. Muchamedov — *Tomsk State University, Russia*

Fault Tolerance of Decomposed PLAs

O. Keren — *Bar Ilan University/School of Engineering, Israel*

I. Levin — *Tel Aviv University/School of Education, Israel*

Thermal Aware Test Scheduling for Stacked Multi-Chip-Modules

Vinay N.S. — *Cisco Systems, Bangalore, India*

Indira Rawat — *Electrical Engineering Dept., Engineering College, Ajmer, India*

M.S. Gaur — *Computer Engineering Dept., Malaviya National Institute of Technology, Jaipur, India*

Erik Larsson — *Linkoping University, Sweden*

Virendra Singh — *Indian Institute of Science, India*

13:30—15:00 **Lunch**

15:00—20:00 **Social Event: Great Peterhof Palace**

20:00—22:00 **Gala Dinner**

Fourth Day: September 20st, 2010 (Monday)

09:00—11:00 **Plenary Session D**
Moderator: Maksim Jenihhin, *Estonia*

09:00—09:30 **Keynote Address:**
Modelling in Hardware Testing
Michel Renovell — *LIRMM, France*



Fourth Day: September 20st, 2010 (Monday)

Invited Talks:

- 09:30—10:00 **Energy-Efficient Fault Tolerance:
A Microarchitectural Solution for Chip
Multiprocessors**
Virendra Singh — *Indian Institute of Science,
India*
- 10:00—10:30 **Modeling faults in reversible circuits**
Iliia Polian, *University of Passau, Germany*
- 10:30—11:00 **Design of Secure Hardware Resistant to the
Attacks**
Mark Karpovsky — *Reliable Computing Laboratory
College of Engineering, Boston University*

11:00—11:30 **Coffee Break**

11:30—13:30 **Session 4-A: CAD and EDA Tools, Methods
and Algorithms**
Moderator: Yegor Vdovychenko

Vector Logic Analysis of Associative Matrices

Vladimir Hahanov, Eugenia Litvinova, Svetlana
Chumachenko — *Kharkov National University of
Radioelectronics (KHNURE), Kharkov*

Wajeb Gharibi — *Jazan University, Kingdom of
Saudi Arabia*

Process Models for Analyzing Associative Data Structures

Hahanov V., Guz O., Ngene Christopher Umerah,
Olhovoy V. — *KHNURE, Kharkov*

Metrics of Vector Logic Algebra for Cyber Space

Vladimir Hahanov, Alexander Mishchenko, Vitaliy
Varetsa — *Kharkov National University of
Radioelectronics, Kharkov*

Cyber Space Evolution

Vladimir Hahanov, Anna Hahanova, Vagan
Zakaryan — *Kharkov National University of
Radioelectronics, Kharkov*



Fourth Day: September 20st, 2010 (Monday)

Logical Method for Detecting Faults by Fault Detection Table

Vladimir Hahanov, Irina Pobizhenko, Tiecoura Yves — *Kharkov National University of Radioelectronics, Kharkov*

Table Data Structures for Cyber Space

Vladimir Hahanov, Eugenia Litvinova, Aleksey Priymak — *Kharkov National University of Radioelectronics, Kharkov*

13:30—15:00 **Lunch**

15:00—16:00 **Symposium Closing – Action hall**

16:00—22:00 **Departure**

Poster Session

Optimization of Sensitivity Dominating Parameters OA in Selective IP Blocks

Sergei G. Krutchinsky — *Taganrog Institute of Technology Southern Federal University, Russia*

Common-mode signal minimization in differential stage

Sergei G. Krutchinsky, Michael S. Tsibin, Alexey E. Titov — *Taganrog Institute of Technology Southern Federal University, Russia*

Linear Devices High Frequency Correction

Sergei G. Krutchisky, Sergey S. Gripinskiy — *Taganrog Institute of Technology Southern Federal University, Russia*

New Method of Multi-Level Optimization

Asadov H.H., Aliyeva Y.N., Bayramova L.A., Ismailov K.Kh. — *National Aerospace Agency, Azerbaijan*



Poster Session

Utilization of Variation Optimization for Location of Emitter of Random Noise Signal

Asadov H.H., Abdullayev N.A., Kerimov M.J., Dadashov E.F. — *National Aerospace Agency, Azerbaijan*

Information Optimization of Distributed Net of Receivers of Acoustic Noise Type Signals

Asadov H.H., Abdullayev N.A., Ibrahimov E.A. Garayev V.M., Abbaszadeh E.F. — *National Aerospace Agency, Azerbaijan*

Optimization of Information – Measuring Systems of Non-Stationary Operational Regime in Multiple Measurements Mode

Asadov H.H., Abdullayev N.A., Agayev I.Kh., Nabyev N.A., Rajabli R.T. — *National Aerospace Agency, Azerbaijan*

On Possibility of Stabilizing Results for Multicriteria Optimizing Linear Combination of Concurrent Functionals

Asadov H.H., Abdullayev N.A., Jalilov S.B., Nabyev N.A., Javadov N.H. — *National Aerospace Agency, Azerbaijan*

Building of the Logic Network of the Information Area of the Corporation

Khairova N., Sharonova N. — *National technical university “Kharkov Polytechnic Institute”, Ukraine*

The Method of a Data Encoding on the Basis of a Punched Lexicographic Rule

Barannik V.V., Shinkarev V.V., Gurzhyi P.N. — *Ukrainian State Academy of Railway Transport, Ukraine*

The Method of Decoded - Firm Presentation Forming of Images in the Systems of the Poliadic Encoding

Barannik V.V., Sidchenko S.A., Larin V.V. — *Ukrainian State Academy of Railway Transport, Ukraine*



Poster Session

Smart Tools for Diagnosis Computer Failures

Krivoulya G.F., Kucherenko D., Dubinsky N. —
*Kharkov National University of Radioelectronics,
Ukraine*

Analysis and Review of the Contribution of Neural Networks to Saving Electricity in Residential Lighting by a Design in MATLAB

Cesar Hernandez, Ricardo Romero, Diego Giral—
Distrital F. J. C. University, Colombia

A New Technique to Improve the Dielectric Strength of a Multi-Dielectric Insulation System

K. Abu-Elabbas — *Academy of Specialized
Studies, Labour university, Egypt*

Surface Flashover of Insulators in Hot Air with Crossed Electric and Magnetic Fields

K. Abu-Elabbas — *Academy of Specialized
Studies, Labour university, Egypt*

On Introducing Built-In Test for Software Components in AADL Models

Valérie-Anne Nicolas — *Université de Brest,
France*

Internal Structure of Software Application for Controlling Devices via JTAG 1149 Interface

Igor Ilyin, Rostislav Grushvitsky — *Russia*

Cluster Computing Framework Based on Transparent Parallelizing Technology

Vitalij Pavlenko — *Odessa National Polytechnic
University, Ukraine*, Viktor Burdeinyi — *Odessa
National University, Ukraine*

Improving Reliability for Bit Parallel Finite Field Multipliers using Decimal Hamming

Nikolaos Mavrogiannakis, Dhiraj K. Pradhan —
University of Bristol, UK

Costas Argyrides — *Oxford Brookes University,
UK*



Poster Session

CTestBench: A Lightweight C-Based Tool for Specification and Functional Verification of Hardware Designs

Alexander Shishkin — *Institute for System Programming of the Russian Academy of Sciences*

Multilevel Modulation Technique Based on Duo-Binary Transmission and Quaternary-Duo-Binary Transmission in Non-Linear Regime

Majed Omar Al-Dwairi, Ziad Alqadi, Majdi T. Oraiqat, Amjad Abujazar — *Al-Balqa Applied University, Jordan*

Development of the Data-Driven Readout ASIC for Microstrip Detectors

Atkin E., Volkov Yu., Klyuev A., Shumikhin V. — *National Research Nuclear University "MEPhI", Russia*

A Digital Implementation of Multi-h CPM Modem

Kulikov G. V., Unger A. U., Suhanov P. G. — *Moscow State Institute of Radioengineering, Electronics and Automation (Technical University) R&D, Russia*

OFDM-based Audio Watermarking for Electronic Radiotelephone Identification

Aleksandr V. Shishkin — *Odessa National Maritime Academy, Ukraine*

Security Risks in Hardware: Implementation and Detection Problem

Alexander Adamov, Vladimir Hahanov — *Kharkov National University of Radio Electronics, Ukraine*

