Minimizing Path Length in Digital Circuits Based on Equation Solving

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Abstract

In this paper, we propose an approach for minimizing path length from primary inputs to primary outputs in digital circuits. A digital circuit is divided into parts and the flexibility for each part is provided by the largest solution to an appropriate FSM equation. We propose sufficient conditions for checking whether one or some output (transfer) functions can be replaced by a simple function of two primary input variables that can be implemented as a single gate. The established conditions become necessary and sufficient conditions for combinational circuits.

1. Introduction

The complexity of digital circuits increases quickly, and thus, the problem of their optimal design with respect to criteria such as reliability, fault-tolerance, minimal number of communication lines, delay, area etc. remains a challenging problem for developing new information technologies. The best approach for the optimization has been shown to be an iterative optimization checking at each step for conformance and improvement. One such approach is based on solving FSM equations under synchronous composition operators, which model interacting FSMs in hardware. In the paper [1], the authors characterized the solvability of a synchronous equation and showed how to effectively compute a largest solution to a solvable equation (any other solution is a reduction of a largest solution). A largest solution to an equation can be viewed as a general solution to the equation and thus, can be viewed as a reservoir for all possible optimizations of a component of interest, from which an optimal component implementation can be chosen. However, the complexity of solving an FSM equation generally is exponential in the number of states. For this reason, a so-called window approach for optimizing digital circuits was proposed in [2]. We iteratively extract a frame of an appropriate size from a given digital circuit and optimize it with respect to the given criteria. The procedure terminates when we are satisfied with the optimization results.

In this paper, when optimizing a frame, we divide the frame into two sequential circuit components and optimize them independently. For each primary output of a circuit component, we check whether length of a path from primary inputs to this output can be reduced and if so, we perform necessary replacements. For the head component of the extracted frame, such checking is based on a largest solution to a corresponding FSM equation while for the tail component a corresponding FSM with external DNCs is used.

The structure of the paper is as follows. Section 1 contains the preliminaries. Section 2 is devoted to the optimization of combinational circuits while Section 3 discusses how to extend the obtained results to sequential circuits. Section 4 concludes the paper.

2. Preliminaries

In this paper, we use a *behavioral (characteristic) function* in order to represent a digital circuit behavior. This function h is defined over input and outputs variables of the circuit and $h(\mathbf{x}, \mathbf{y}) = 1$ if and only if the circuit produces the output vector $\mathbf{y}$ to the input vector $\mathbf{x}$. Correspondingly for a combinational circuit the behavioral function is specified over input and output variables, while for a sequential circuit the behavioral function is specified over input and output variables as well as state variables of the current and the next state.

2.1.Behavioral function

Consider the combinational circuit in Figure 1.a. The circuit implements a system of Boolean functions Φ (an SBF Φ) and can be described by a corresponding behavioral function $\Psi_\Phi(x_1, \ldots, x_n, y_1, \ldots, y_k)$: $\Psi_\Phi(X_1, \ldots, X_n, Y_1, \ldots, Y_k) = 1$ if and only if $Y_1 = \varphi_1(X_1, \ldots, X_n), \ldots, Y_k = \varphi_k(X_1, \ldots, X_n)$. We say that a function Ψ is an SBF-behavioral function if Ψ is a behavioral function of some system of Boolean, and possibly non-deterministic, functions. Given a Boolean function θ, we denote M_θ^1 the set of variable values, for which the function equals 1. Given Boolean functions θ and Ψ such that $M_\theta^1 \subseteq M_\psi^1$, we denote this fact as $\theta \leq \Psi$.

According to the sequential circuit in Figure 1.b, the behavioral function h is specified over the set $X \cup P \cup Z \cup Y$ of variables and $h(\mathbf{x}, \mathbf{p}, \mathbf{z}, \mathbf{y}) = 1$ if and only if the current state of the registers is $\mathbf{p}$, the input is $\mathbf{x}$, the next state of the registers is $\mathbf{z}$ while the output of the circuit is $\mathbf{y}$.

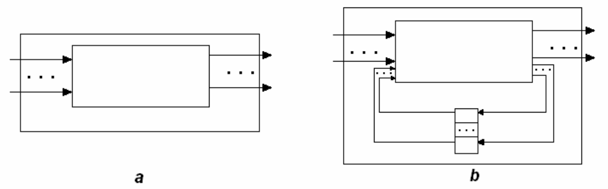

Figure 1. Combinational (a) and sequential (b) circuits

When the initial state of registers is known, generally, not each state is reachable from the initial state. Moving iteratively from state to state we can define an output sequence for each input sequence that is called *output response* of the circuit to a corresponding input sequence. Two circuits are *equivalent* if their output responses at the initial states coincide for each input sequence.

In Table 1 we present two sequential circuits as structural Finite State Machines (FSMs) with the initial states 00 and 0 and for the sake of simplicity, we keep only reachable states in the FSM representation. The part of the behavioral function related to the reachable states can be easily extracted from such representation. FSM C_1 is specified over input variable x and output variables u_1u_2, while the values of the variables p_1, p_2 and z_1, z_2 represent a current and the next state of the circuit. FSM C_2 is specified over input variables u_1 and u_2 and output variable y, while the values of the variables a and b represent the current and next states of the circuit. For example, the behavioral function $\Psi_2(00010) = 1$ while $\Psi_2(00000) = 0$.

Table 1a. FSM C_1

u_1u_2 \ a	0	1
00	1/0	1/1
01	0/1	1/1
10	1/1	0/1
11	0/1	0/1

Table 1b. FSM C_2

x \ p_1p_2	00	01	10
0	01/00	10/01	10/00
1	10/01	00/10	01/00

2.1. The sequential composition of digital circuits

We now consider the sequential composition of two digital circuits (Figure 2) represented by their behavioral functions $\Psi_1(\mathbf{x}, \mathbf{p}, \mathbf{z}, \mathbf{u})$ and $\Psi_2(\mathbf{u}, \mathbf{a}, \mathbf{b}, \mathbf{y})$. The composition is a structural FSM that describes the behavior of the overall circuit. Thus, the behavioral function $\Psi(\mathbf{x}, \mathbf{p}, \mathbf{z}, \mathbf{a}, \mathbf{b}, \mathbf{y})$ of the overall circuit is $(\Psi_1 \wedge \Psi_2)_{\downarrow \mathbf{x},\mathbf{p},\mathbf{z},\mathbf{a},\mathbf{b},\mathbf{y}}$, where $\downarrow_{\mathbf{x},\mathbf{p},\mathbf{z},\mathbf{a},\mathbf{b},\mathbf{y}}$ is the projection of $(\Psi_1 \wedge \Psi_2)$ onto the set of variables $X \cup P \cup Z \cup A \cup B \cup Y$. In this paper, given a Boolean function φ over the set $V \cup U$ of variables, we assume that the set M^1 of the projection $\varphi_{\downarrow \mathbf{v}}$ is the V-projection of the set M_φ^1.

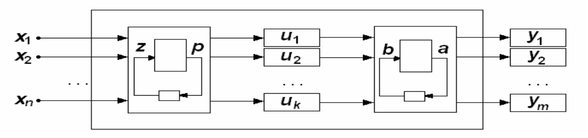

Figure 2. The sequential composition of two circuits

Consider two sequential circuits represented by their structural FSMs in Table 1. We derive the structural FSM $C_1 \bullet C_2$ that is specified over input variable x and output variable y, while the values of the variables p_1, p_2, a and z_1, z_2, b represent the current and next states of the circuit. FSM $C_1 \bullet C_2$ in Table 2 describes the behavior of the sequential composition of C_1 and C_2 with respect to the states which are reachable from the initial state.

Table 2. The structural FSM (only reachable states are shown)

x \ $p_1 p_2 a$	000	011	100	101
0	011/0	101/1	101/0	101/1
1	100/1	000/1	011/0	011/1

In order to optimize the head or the tail component of the composition we should replace a circuit component with another one, such that the external behavior of the overall composition is preserved. All such behaviors can be captured by a largest solution to a corresponding FSM equation [1]. An optimal circuit (according to criteria of interest) can be then extracted from a largest solution. In this paper, for each circuit component, we examine if it is possible to reduce length of paths from primary inputs to primary outputs and correspondingly to reduce path delays. For sequential circuits we are interested in shortening paths from primary inputs and register outputs to primary outputs and register inputs. We first discuss how the problem can be solved for combinational circuits and then extend the obtained results to sequential circuits.

3. Optimizing a combinational circuit

In this section, we assume that components of the sequential composition are combinational circuits. The head component implements the SBF Φ_1; the behavioral function Ψ_{Φ_1} of the head component is specified over the set $\{x_1, \ldots, x_n, u_1, \ldots, u_k\}$ of variables. The tail component implements the SBF Φ_2 and the behavioral function Ψ_{Φ_2} of the tail component is specified over the set $\{u_1, \ldots, u_k, y_1, \ldots, y_m\}$ of variables. The behavioral function Ψ_Φ of the overall circuit which implements the SBF $\Phi = \Phi_2(\Phi_1)$ is specified over the set $\{x_1, \ldots, x_n, y_1, \ldots, y_m\}$ of variables and $\Psi_\Phi = (\Psi_{\Phi_1} \wedge \Psi_{\Phi_2})_{\downarrow \mathbf{x}, \mathbf{y}}$.

3.1. Solving an equation over the head component

The set of all behaviors which can replace the head component is captured by the largest solution of an FSM equation and can be determined using the following statement:

Proposition 1. Given SBF

$$\Phi_3 = \begin{cases} u_1 = \theta_1(x_{1,\ldots,}x_n) \\ \quad\ldots\ldots\ldots\ldots \\ u_k = \theta_k(x_{1,\ldots,}x_n) \end{cases},$$

$\Phi_2(\Phi_1) = \Phi_2(\Phi_3)$ if and only if $\Psi_{\Phi_3} \le \overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}}$, where $\overline{\varphi}$ is the inversion of the function φ.

Proposition 1 gives a guide how to determine an SBF that can replace SBF Φ_1 without changing the behavior of the overall system. In this section, we illustrate how to check whether one or more functions of the head component can be selected as functions of two input variables.

First, we briefly sketch the method in [3] how to check whether one or more functions of the head component can be selected as functions equal to the constant 1 (or to the constant 0).

In this case, given a function $\overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}}$, we are required to check if there exists a system Φ_3 of Boolean functions $\theta_1(x_1, \ldots, x_n)$, …, $\theta_k(x_1, \ldots, x_n)$, where the function θ_j equals the constant 1, and $\psi_{\varphi_3} \le \overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}}$. We can determine such an SBF Φ_3 using the conjunction of the function $\overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}}$ and the variable u_j. The following statement holds:

Proposition 2 [3]. There exists SBF Φ_3, $\Psi_{\Phi_3} \leq \overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}}$, such that the function θ_j equals to the constant 1 if and only if the function $(\overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}} \wedge u_j)_{\downarrow x}$ equals to the constant 1.

The proof is implied by the fact that for each input pattern **x** there should exist the pattern **u** of internal variables u_1, u_2, …, u_k where $u_j = 1$, such that the function $\overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}}$ equals 1 for the pattern **xu**.

We note that Proposition 2 can be easily transformed for checking whether there exists an SBF Φ_3 where an appropriate function equals the constant 0. In this case, we need to project the function $(\overline{u_j} \wedge \overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}})$ onto the set $\{x_1, x_2, \ldots, x_n\}$ of variables.

We use an example from [3] to demonstrate how Proposition 2 can be used for the optimization. We consider a combinational circuit represented in Figure 3.

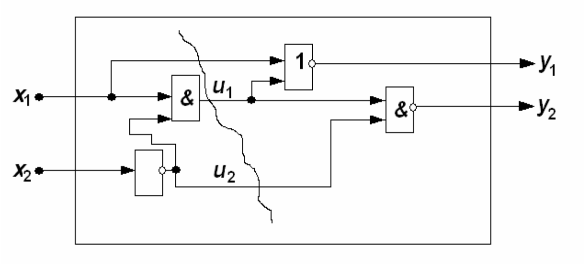

Figure 3. Initial combinational circuit

The functions can be calculated based on the cut of the circuit (Figure 3). In this case, $\overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}} = \overline{x_1}\,\overline{u_1} \vee x_2\overline{u_1} \vee x_1\overline{x_2}u_1u_2 \vee x_1x_2u_1\overline{u_2}$. The conjunction of this function and the function u_2 equals $\overline{x_1}\,\overline{u_1}u_2 \vee x_2\overline{u_1}u_2 \vee x_1\overline{x_2}u_1u_2$. It means that for input patterns **x** = 00, 01, 11 we can select u_1 and u_2 as 11 and there exists SBF Φ_3, $\Psi_{\Phi_3} \leq \overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}}$, such that the function $u_2 = \theta_2(x_1, x_2)$ equals the constant 1. We note that $u_1 \wedge 1 = u_1$ and the NAND gate can be replaced by an inverter. The optimized combinational circuit is shown in Figure 4.

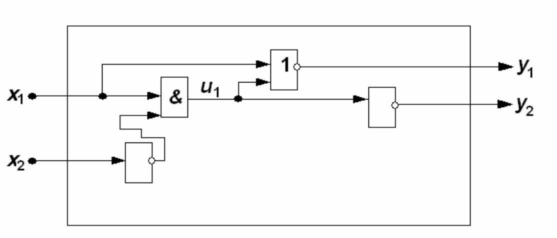

Figure 4. The combinational circuit after optimization

We now consider all the output functions of the head circuit and select a function θ_j that has the longest sequence of gates from primary inputs to the corresponding output. Let $p(x_i, x_r)$ be a function of two primary inputs x_i and x_r. Usually $p(x_i, x_r)$ is selected in such a way that it can be implemented by a single gate. For example, $p(x_i, x_r)$ can be the conjunction of two variables, the disjunction of two variables, etc. In order to check whether a corresponding output function of the head circuit component can be replaced by $p(x_i, x_r)$, we add a new variable $u_{k+1} = u_j \oplus p(x_i, x_r)$. In this case, there exists SBF Φ_3, $\Psi_{\Phi_3} \leq \overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}}$, such that the function θ_j equals to $p(x_i, x_r)$, if and only if there exists such a system where θ_{k+1} equals to the constant 0. Thus, the following statement holds:

Proposition 3. There exists SBF Φ_3, $\Psi_{\Phi_3} \leq \overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}}$, where $u_j = p(x_i, x_r)$, if and only if there exists SBF Φ such that u_{k+1} equals to the constant 0 and $\Psi_\Phi \leq (\overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_\Phi})_{\downarrow \mathbf{x},\mathbf{u}}})_{\downarrow \mathbf{x},\mathbf{u}} \wedge (u_{k+1} = u_j \oplus p(x_i, x_r))$.

Trying all the primary outputs of the head circuit component and all possible functions which correspond to available gates with two inputs, we can say whether there exists such an SBF that the sequence of gates to a corresponding primary output can be replaced by a single gate.

3.2. Solving an equation for the tail component

The set of all behaviors of the tail component can be captured by a partial FSM that is defined only for *u*-patterns which can be output patterns of the head component. Thus, in order to get *u*-inputs where the behavior of the tail component cannot be changed we take the projection $(\Psi_{\Phi_1} \wedge \Psi_{\Phi_2})_{\downarrow \mathbf{u},\mathbf{y}}$. This function is not really a behavioral function, since it describes only a part of behavior. If for some *u*-pattern there is no *y*-pattern in the set M_{ψ}^{1} then the behavior of the tail component for this *u*-pattern can be selected in an arbitrary way (so-called input don't care conditions). We consider again a function $p(u_i, u_r)$ of two input variables u_i and u_r. Let

$$\Phi_2 = \begin{cases} y_1 = \omega_1(u_{1,\dots,}u_k) \\ \dots\dots\dots\dots \\ y_m = \omega_k(u_{1,\dots,}u_k) \end{cases}.$$

Given a function $\Psi(u_1, \dots, u_k, y_1, \dots, y_m)$, $\Psi = (\Psi_{\Phi_1} \wedge \Psi_{\Phi_2})_{\downarrow \mathbf{u},\mathbf{y}}$, it holds that $\Psi \le \Psi_{\Phi_2}$. We replace the variable y_j in Ψ by the function $p(u_i, u_r)$ and obtain the function Ψ_p over the same set of variables.

Proposition 4. There exists SBF Φ_3 such that the function ω_j equals $p(u_i, u_r)$ and $\Phi_3(\Phi_1) = \Phi_2(\Phi_1)$ if and only if $\Psi \le \Psi_p$.

The proof is implied by the fact that for each input pattern **u** that can be produced by the head component, it holds that $y_j = p(u_i, u_r)$; thus, the function ω_j can be replaced by the function $p(u_i, u_r)$ without changing the external behavior of the overall circuit.

3.3. Experimental results

We experimented with the proposed method on some benchmarks [4] in order to see how often given a combinational circuit, we can reduce the length of a path from primary inputs to primary outputs for a given circuit. For each benchmark, at the first step we extract a frame (a combinational circuit) of an appropriate size that has up to 20 inputs where path length from primary inputs to primary outputs is 7-8 on average while being up to 18-24 for some benchmarks. We divide the extracted frame into two parts and for each circuit component we check whether some paths could be shortened. We use ten functions of two variables, such as AND, OR, etc., which can be easily implemented by a single gate. We take several cuts of the same circuit and check each of them. Our results clearly show that on average 20% of internal and external outputs can be implemented as a single gate that depends on two variables. For some frames of some benchmarks the number of such outputs reaches 33%. If such an optimization is performed for the tail component then we add an appropriate gate and delete all the gates of the corresponding path which do not influence other outputs. Correspondingly, the number of gates of the overall circuit can also be reduced.

4. Optimizing components of a sequential circuit

We now assume that components in Figure 1 are sequential circuits, i.e., they have registers (state variables). The behavior of the composition can be described in the same way as the appropriate projection of the conjunction of the component behavioral functions. A largest solution to an appropriate FSM equation is also constructed in the same way. However, the problem how to analyze this largest solution is much more complex according to the following reasons. First of all, the largest solution can have states where the behavior is not specified for some inputs; this means that if a circuit component reaches a corresponding state then these inputs cannot be applied without violating the external behavior of the overall circuit. Such states must be iteratively deleted from the largest solution and the procedure of deleting this part from a behavioral function is rather complex. For this reason, we consider only a part of the largest solution that preserves the transition function of the head circuit component.

For the head component we obtain the behavioral function $\overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_{\Phi}})_{\downarrow \mathbf{x},\mathbf{p},\mathbf{z},\mathbf{a},\mathbf{b},\mathbf{u}}}$ of the largest solution. In order to keep consistency between the transition functions of the initial and modified components, we project the behavioral function of the head component onto input and state variables and derive the conjunction of the projection with the function $\overline{(\Psi_{\Phi_2} \wedge \overline{\Psi_{\Phi}})_{\downarrow \mathbf{x},\mathbf{p},\mathbf{z},\mathbf{a},\mathbf{b},\mathbf{u}}}$. If we use information about states that are unreachable from the initial state, then the obtained formula has the complete flexibility for the head component when the transition function of the initial head component is preserved. At the next step, we apply the results of Section 3.1 in order to check if one or several transition and/or output functions of the head component can be replaced by the function that is equal to constant 1 (or 0), or can be replaced by a single function of two input variables such as conjunction, disjunction, etc.

For the sequential composition of circuits in Table 1 we obtain the behavioral function represented by a structural FSM in Table 3.a (transitions for unreachable states are not shown).

Table 3a. The flexibility of FSM C_1

x \ $p_1 p_2$	00	01	10
0	01/00	10/00,01	10/00
1	10/01,11	00/10,11	01/00

Table 3b. The flexibility of FSM C_2

$u_1 u_2$ \ a	0	1
00	1/0	1/1
01	0/1	11
10	-	0/1
11	-	-

When optimizing the tail component, we project the function $(\Psi_{\Phi_1} \wedge \Psi_{\Phi_2})$ onto input, state and output variables of the tail component and apply the results of Section 3.2 in order to check if one or several transition and/or output functions of the tail component can be replaced by the function that is equal to constant 1 (or 0), or can be replaced by a single function of two input variables such as conjunction, disjunction, etc.

For the sequential composition of circuits in Table 1 we obtain the behavioral function represented by a structural FSM in Table 3.b, where the notation "-" represents unspecified transitions.

5. Conclusions

In this paper, we have proposed how to optimize a digital circuit by dividing the circuit into two sequential circuit components. Each circuit component is optimized independently. Using the flexibility provided by a largest solution to an appropriate FSM equation, we propose sufficient conditions for checking whether one or some output (transfer) functions can be replaced by a function equal to the constant 1 (or 0), and/or by a simple function of two input variables that can be implemented as a single gate. Such replacement can shorten a path from primary inputs to primary outputs in a circuit component and correspondingly in the overall circuit. In turn, it can imply the deterioration in the number of gates. The established conditions become necessary and sufficient conditions for combinational circuits. We also note that all the checks can be performed fast enough when BDDs [5] are used for behavioral function representation. Another way to speed-up checking is to use interpolants and appropriate SAT-solvers [6].

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References:

[1] N.Yevtushenko, T.Villa. R.K.Brayton, A.Petrenko, A.Sangiovanni-Vincentelli Logic synthesis by equation solving// In Proc. Of the XVI Intern. Workshop on Logic synthesis, 2000, P. 11-14.

[2] S.Zharikova, M.Vetrova, N.Yevtushenko Optimization of a multi component digital circuit by solving a system of FSM equations // Proceedings Euromicro Symposium on Digital System Design Architectures, Methods and Tools, IEEE Computer Society. – Belek-Antalya, Turkey. – 2003. – pp. 62-68.

[3] N.Kushik, M.Reckun Optimization of combinational circuits based on equation solving// Vestnik of Krasnoyarsk University, 2008 (submitted for publication).

[4] Education: Virginia Tech: The Bradley Department of Electrical & Computer Engineering / College of Engineering; ISCAS89 Sequential Benchmark Circuits. – Access mode to an electronic resource. http://www.ece.vt.edu/mhsiao/iscas89.html is free.

[5] CUDD [Electronic resource] – http://vlsi.colorado.edu/~fabio/CUDD/

[6] Kenneth L. McMillan Interpolants and Symbolic Model Checking. VMCAI, 2007, P. 89-90.