

Digital Lock Detector for Phase Locked Loop

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Abstract

The purpose of this work is to add one more circuit into the traditional PLL [1] to define the lock condition. Fully digital lock detector is presented. Presented circuit provides a simple design, process independence and design automatation.

1. Introduction

It is known [1] that the traditional phase locked loop (PLL) generally consists of 4 parts (Figure 1), where PFD is the phase-frequency detector, CP-LPF is the charge pump and the low pass filter together, VCO is the voltage controlled oscillator, Fref is the PLL reference signal, Ffb is the PLL feedback signal, Fout is the output signal. PFD compares the phases of reference and feedback signals. The PFD generates an output signal, proportional to the phase difference between the Fref and the Ffb. This signal is filtered by the CP-LPF. The filtered signal is connected to the input of the VCO. Divider is used to divide the output signal of the PLL and to realize the feedback. When the phases of the ref and the fb signals are equalized, the voltage on loop filter (control voltage) stabilizes. It means that the PLL is in lock condition.

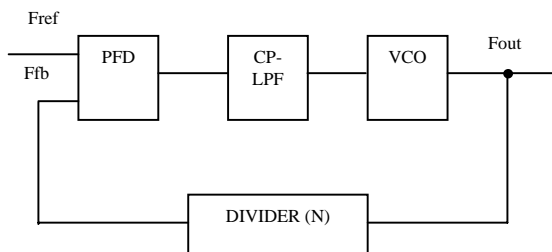


Figure 1. Block diagram of traditional PLL

2. Considered scheme

In [2-4] analytical calculations for different lock detectors can be found. In this work design solution is presented. In [8] analog lock detectors are presented. As it was mentioned, in this work only a digital lock detector is considered (Figure 2.).

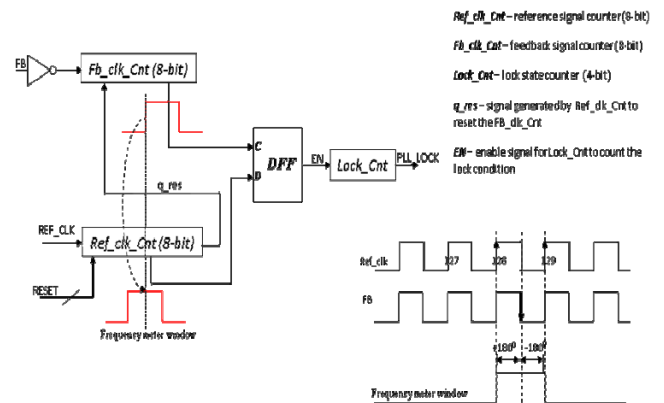


Figure 2. Block diagram of digital lock detector

The Ref_clk_Cnt and the Fb_clk_Cnt are N-bit binary counters (the same counters, in this case $n=8$) (Figure 2). DFF compares the values of these two counters. The Lock_Cnt is an M bit counter.

The operation is based on the comparison of equality of frequencies of reference and feedback signals. First the circuit is reset. Then the Ref_clk_Cnt and the Fb_clk_Cnt begin to count independently from each other. After every 2^{n-1} cycles the state of Fb_clk_Cnt is being compared with the state of Ref_clk_Cnt (with DFF). After every 2^n cycles

Ref_clk_Cnt generates q_res signal to reset the Fb_clk_Cnt. If the frequencies of Ref_clk and Fb are equal, EN signal enables the Lock_Cnt to count. The most significant bit of Ref_clk_Cnt is given to Lock_Cnt as clock. While the EN is active (logical "1"), the Timer continues to count until it gets to its maximum value. Afterwards the circuit shows that the PLL is in lock condition (PLL_LOCK="1"). When the PLL is in and the values of Ref_clk_Cnt and the Fb_clk_Cnt become non-equal, the EN signal switches to "0". While the EN is equal to "0", the Lock_Cnt counts to fix the time, in which the PLL comes out from lock condition. When the Timer counts up to a some defined value, PLL_LOCK is set to "0". It means the PLL is in unlock condition.

3. Results

Gate level RTL code is written for the digital lock detector (in Verilog HDL). It means that the design is technological process-independent, it can be implemented by the EDA tools. So if there is an RTL code and the design flow has been developed once, the design of the digital lock detector can be done in a short time. This is one of the main advantage of the digital lock detector. The other advantages compared with the digital lock detector, presented in [8] is the low power consumption (almost 5 times) and the smaller area.

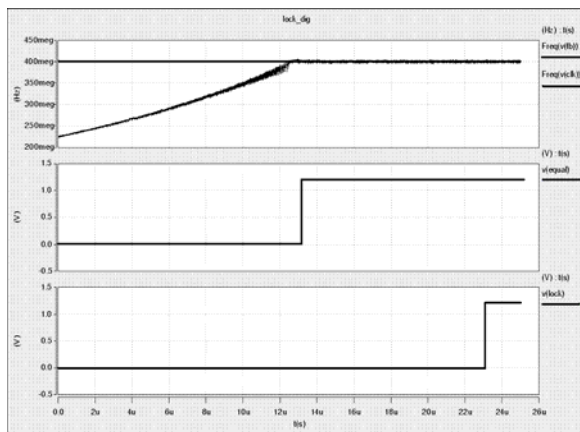


Figure 3. Simulation results of lock detector

Simulation results for lock detector are shown in Figure 3. On the top the frequencies of reference and feedback signals are shown. The Lock_Cnt EN signal is shown in the middle and the PLL_LOCK signal in

the bottom. As it can be seen (Figure3.), PLL_LOCK signal become active (logical "1") after 10us after the EN signal (4096 reference clock cycles). This value is connected with the resolution of the counters.

4. Conclusion

The main advantage of digital lock detector is the process independence, design simplicity. The digital lock detector, considered in this paper, has less current consumption, than the one presented in [8]. This design can be implemented by EDA tools.

6. References

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