

Performance Evaluation of In-Circuit Testing on QCA based Circuits

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Abstract

Quantum-Dot Cellular automata based circuits (QCA) are one of the favorite novel technologies, which operates on binary data at the nanometer-scale; in which logical operations and data movement are accomplished via Columbic interaction rather than electric current flow leading to a very little power dissipation. Since circuits made from QCA devices could provide various “wins” over CMOS, in recent years there has been an influx of QCA-related research. However before implementing every circuit, its testability and reliability must be mentioned. Hence, testing of these devices is our main concern in this paper and we will show how to perform In-Circuit-Testing on them and the differences and difficulties which is caused by the quantum entity of these circuits.

1. Introduction

Electronic devices are designed in different sizes and schemes to perform better services. Referring to vital servicing without any malfunctioning in these systems, testing is one of the main principles for them. Test procedure contains applying input patterns to the circuit under test (CUT) and receive the practical outputs simultaneously and then compare them with expected vectors as shown in Figure1.

Different ways of applying test inputs vectors to CUT causes different approaches and methods in this field such as exhaustive /pseudo exhaustive testing, pseudo random testing, and deterministic testing. Testers are divided into two main species: *functional* testing and *in-circuit* testing.

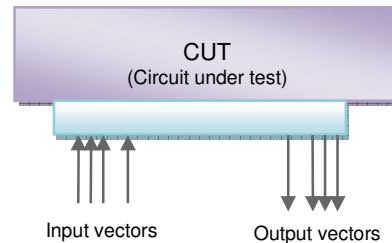


Figure 1. Principles of test procedure

Functional testers try the CUT in a way similar to its use in the main system and are subdivided into static and dynamic which in respect, are *CPU rate dependable* and *clock rate* tester. On the other hand in-circuit testing uses a *printed circuit board* and tests each segment independently.

According to the recent research, Conventional CMOS technology seems to be superseded by nano scale technologies which can achieve a density of 10^{12} devices/cm² and operate at THZ frequencies.

Among these new devices, Quantum-dot Cellular Automata (QCA) offers a solution at nano scale, and also provides a new method of computation and information transformation [1].

QCA is attracting lots of attentions due to its extremely small feature size and ultra low power. The unique specification of QCA based designs is that logic states are represented by the position of individual electrons and are not stored in voltage levels as in CMOS based designs.

A common quantum dot cell shown in Figure 2 consists of four dots at the corners with two excess electrons that can tunnel between the dots. Due to

Coulomb repulsion, the two excess electrons always occupy diagonally opposite dots.

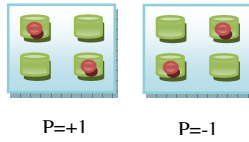


Figure 2. A Quantum-dot cellular automaton with different polarization.

The repelling Coulomb force between electrons exists also between adjacent cells. Two adjacent cells always assume a position where the columbic repulsion is minimum. This principle causes the cell to have a desired logic obliged by its adjacent cells.

The basic logic elements of QCA-based designs are different from conventional CMOS circuits. E.g. the majority gate is one of the basic logic elements in the technology as shown in Figure 3(a). Therefore new testing schemes are required for this technology.

The main question in testing area of QCA circuits is that whether we could obey the same rules in CMOS based circuits or not. Faults in CMOS circuits can be mostly modeled by SSF-stack at faults.

The three most common defects which are specially belongs to QCA circuits are *displacement*, *misalignment* and *omission*, which are shown in Figure 3(b), 3(c), 3(d) respectively.

In a cell displacement defect, the defective cell is displaced from its original position (Figure 3(b)). In a cell misalignment defect, the direction of the defective cell is not properly aligned (Figure 3(c)). In a cell omission defect (Figure 3(d)), the defective cell is missing as compared in the case (a).

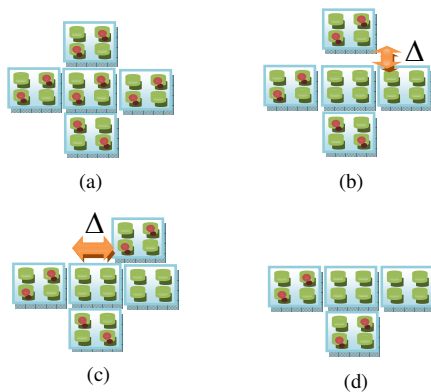


Figure 3. (a) Majority function implemented in QCA, QCA defects: (b)displacement, (c) misalignment, (d) omission.

Lots of work is done on these topics and many solutions are represented but as this field is new, simulation axes are limited. Here software QCADesigner 2-0-3 is used. In this paper we employ the well known testing methods on these circuits and figure out whether they are preferable or not.

The rest of the paper is organized as follows: Section 2 discusses the related work in this field. Section 3 describes the design flows of functional and in-circuit testers and also implementation and synthesis steps are presented, while section 4 provides experimental results and section 5 concludes the paper.

2. Related work

To consider the dimensions associated with the QCA technology and compare them with conventional CMOS, [4] is a good reference. In [3] the first comprehensive majority/minority network synthesis methodology for multi-level networks targeted at QCA devices is presented and the first majority network synthesis tool is produced. As represented in [2], a 100% single stuck-at fault test set for designs mapped into QCAs does not necessarily detect all stuck-at faults in majority voters. In [2], testing of QCA based designs is studied and unique testing properties of this technology have been identified.

3. Design flow and Implementation

In-circuit testing is an approach in which it is possible to contact with the UUT, and testing them by sending motives and receiving and evaluating the results with the correct known board outputs. The in-circuit testing diagram is shown in Figure 4.

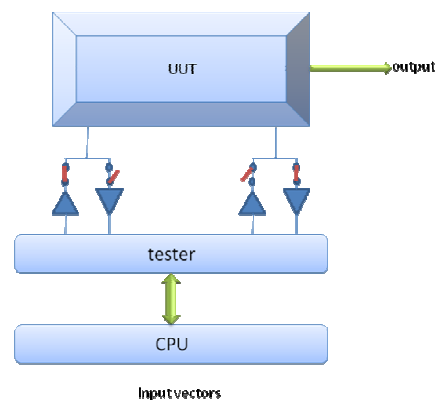


Figure 4. In-circuit testing diagram

Obviously there are some notices to mention such as flow repulsion which occurs when the node on the UUT obliged to have a logic level different from the accurate level. The same idea is done on a sample circuit shown in Figure 5.

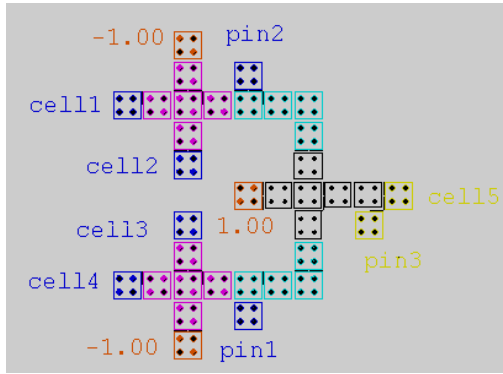


Figure 5. Simulating the In-circuit testing on a certain circuit.

The circuit consists of two *or* gates and one *and* gate. Cell 1, 2, 3 and 4 are the input cells and cell 5 is the output of this circuit. Pin1, 2, and 3 are considered as probes. Here, the goal is to test the *and* gate as a node. The simulation results are shown in Figure 6. Various experiments have been done on the same circuit and different results are extracted. If the circuit works properly the results will be the same as the good-known board output.

The main principle which influences the results is *QCA clocking* concept. In general, a clocked QCA design uses four clocks; each clock is 90 degrees out-of-phase from its previous clock. *Switch, hold, release* and *relax* are their four phases. In Figure 5 different cells of different colors; blue, pink, green and black are shown, indicating their phases. The phase of the adjacent cell affect pin. Some cells in different phases cannot be selected for locating a pin.

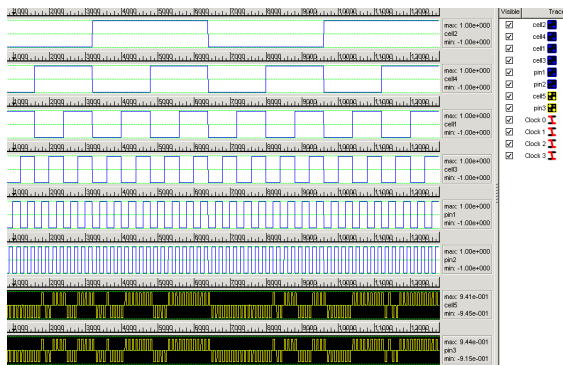


Figure 6. Simulation results of the circuit of Figure 5.

At smaller clock pulses, putting the pins on farther cells will reduce the punctuality. In other words, increasing the number of cells between ideal location and possible locations influence the results.

4. Experimental Result

Table 1 indicates the condition of simulation and the experimental results.

Table 1: experimental results of the two simulations as a sample (Clock: min=9.80e-022, Max=3.80e-023)

Cell5 (output)	Pin3 (probe)
$\pm 9.34e-001$	$+9.80e-022,$ $-3.80e-023$
$\pm 9.34e-001$	$\pm 9.79e-001$

The results show that the *and* gate is acting correctly.

5. Conclusions and Future Work

As a matter of fact, the main concern of designers before fabrication and manufacturing will be the testability of circuits and leading to have reliable design. In-circuit testing as one the well known methods of testing is examined on QCA circuits in this project. The simulation results show that since the distance is a main factor of these circuits, determination of the favorite location of the cell which plays the role of the probe is sensitive. QCA clocking principle is also effective and each probe has to be on the cell in desirable phase to have the accurate result. Evaluating other methods of testing such as short-circuit testing, open-circuit testing, etc. can be accomplished in the future researches on these circuits.

6. References

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