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CONTENTS

Modeling of Frequency Conversion in a Chain of Coupled Resonators due to Time Change in Permittivity

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***Abstract* — This paper considers the transformation of natural modes of single and coupled dielectric resonators when their material is subject to an abrupt time change in permittivity. Both the transient response and the new steady state regime are described in detail. Possibility of frequency shift is demonstrated. Enhancement of the frequency shift for the coupled modes with odd-odd symmetry in the chain has been shown.**

***Index Terms* — Dielectric resonators, time-varying media, whispering gallery modes.**

I. Introduction

Dielectric resonators with whispering-gallery modes (WGM) have been the subject of significant interest in recent years as they exhibit properties useful for a wide range of applications, including low-threshold lasers [1], ultra-small filters [2] and sensors [3, 4]. However, much of the theoretical work focused upon resonators has concentrated upon prediction of their frequency domain properties, although accurate time domain modeling is essential for microwave design, especially for active devices and circuit components.

The most widely used today numerical approach is FDTD method that is flexible but demands large computer memory. Moreover, conventional FDTD codes have problems with visualization of the high Q resonances.

In this paper we use rigorous mathematical method that allows us to analyze problems both in the frequency domain and in the time domain. Applying the Laplace transform directly to the wave equation we derive an analytical solution of the problem in the frequency domain. Then we recover the time domain electromagnetic field by virtue of the computation of the inverse Laplace transform via the residue evaluation at singular points associated with eigenvalues of the structure. This approach guarantees accurate back transformation with controllable accuracy and allows us to extract and interpret physical phenomena easily. This method has been already successfully applied to a variety of time domain problems with different geometries [5-7].

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In this paper we investigate the transient response of a WGM of the resonator to an abrupt change in permittivity. Proposed approach is extended then to the case of WGM transformation in a finite linear chain of coupled circular dielectric resonators due to temporal changes in their permittivity. In practice, temporal changing of the material constants index can be realized by varying an input signal in a nonlinear structure [8]; by voltage control [9]; by a focused laser beam as a local heat source [10] or else by a plasma injection [11]. Note that the temporal variations of the permittivity of an unbounded medium transform the frequency of an existing monochromatic field, however both the wavenumber and the field pattern are conserved [12, 13].

In this paper, the details of the field evolution during the transient period in a single resonator and in a linear chain of coupled resonators will be characterized.

II. Mathematical Formulation

A. Single resonator

We consider a circular dielectric resonator of radius a. This can be viewed as a 2D model of a thin-disk 3D resonator within the effective refractive-index approximation. Dielectric permittivity of the material is ε_1, surrounding medium is a vacuum. The material is considered to be linear and non-magnetic. To describe the fields, the cylindrical system of coordinates ρ, φ, z, centered on the resonator, is introduced. Before a change in the permittivity, an initial field exists in the resonator which is an H-polarized natural mode as this type of modes is dominant in thin disks; the z-component of it can be represented in the following form

$$H_z = A\begin{cases} b_k J_k(k_1\rho)\cos k\varphi, & \rho < a \\ H_k^{(2)}(k_0\rho)\cos k\varphi, & \rho > a, \end{cases} \qquad (1)$$

wher $b_k = H_k^{(2)}(k_0 a)\big/J_k(k_1 a)$, $k_0 = \omega_0/c$, $k_1 = \sqrt{\varepsilon_1}\,\omega_0/c$, c is light velocity in vacuum, ω_0 is complex valued eigenfrequency that is the solution of the equation

$$J_k(k_1 a)H_k'^{(2)}(k_0 a) - \frac{k_0}{k_1}J_k'(k_1 a)H_k^{(2)}(k_0 a) = 0 \qquad (2)$$

The time dependence is assumed as $e^{i\omega_0(t-t^*)}\Theta(t-t^*)$, where $t^* < 0$ is the moment of switching on the mode. At zero moment of time the dielectric permittivity inside the resonator changes abruptly in value from ε_1 to ε_2 in response to an external force. We now investigate the mechanisms that couple the initial mode to those of the cavity with the new permittivity, with particular emphasis on the transient processes occurring in such a single dynamic resonator. The formulation of the problem in the above manner permits construction of an analytical solution that explains the interesting phenomena in detail.

The transformed field has to satisfy the wave equations

$$\begin{aligned} &\Delta H - \frac{\varepsilon_2}{c^2}\frac{\partial^2}{\partial t^2}H = 0, \ \rho < a, \\ &\Delta H - \frac{1}{c^2}\frac{\partial^2}{\partial t^2}H = 0, \ \rho > a. \end{aligned} \tag{3}$$

Here H represents H_z component of the field which is perpendicular to the plane of the resonator and Δ is the Laplace operator

$$\Delta = \frac{\partial^2}{\partial\rho^2} + \frac{1}{\rho}\frac{\partial}{\partial\rho} + \frac{1}{\rho^2}\frac{\partial^2}{\partial\varphi^2}.$$

We apply the Laplace transform

$$L(p) = \int_0^\infty W(t)e^{-pt}dt$$

directly to the wave equation (3).

The electric field flux density, as well as the magnetic induction, remains continuous at time jumps of the medium parameters. It follows that the initial conditions in transient region have the form

$$H(t=0^+) = H(t=0^-), \ \frac{\partial}{\partial t}H(t=0^+) = \frac{\varepsilon_1}{\varepsilon_2}\frac{\partial}{\partial t}H(t=0^-). \tag{4}$$

Here we adopt the evolutionary approach presented in [6]. Within this approach, the complete transient solution is explicitly constructed as a superposition of the waves reflected from the structure boundaries; the field at an instant just after the moment of switching being evaluated as if the transient medium is unbounded. Therefore, because of the finite speed of the electromagnetic waves, the influence of the resonator boundary appears only after a finite time delay from the moment of switching and this will be discussed further.

We will seek the solution in the form

$$\begin{aligned} L_{in}(p) &= Ab_k \cos k\varphi \frac{v_1^2 p + i\omega_0 v_2^2}{p^2 v_1^2 + \omega_0^2 v_2^2} J_k(k_1\rho)e^{-pt^*} + \\ &+ \cos k\varphi B_k(p) I_k\left(\frac{p}{v_2}\rho\right), \ \rho < a \end{aligned} \tag{5}$$

$$\begin{aligned} L_{out}(p) &= A\cos k\varphi H_k^{(2)}(k_0\rho)\frac{e^{-pt^*}}{p - i\omega_0} + \\ &+ \cos k\varphi C_k(p) K_k\left(\frac{p}{c}\rho\right), \ \rho > a, \end{aligned} \tag{6}$$

where $v_1 = c/\sqrt{\varepsilon_1}$, $v_2 = c/\sqrt{\varepsilon_2}$. The complete field within the cavity consists of the unbounded term (first term in (5)) and additional contributions due to the boundary. Similarly, in the outer region the field comprises a superposition of the initial field (first term in (6)) and contributions due to the presence of the boundary.

Outside the cavity, the function $K_k(..)$ guarantees satisfaction of the Sommerfeld outgoing radiation condition at infinity, and B_k and C_k are unknown coefficients to be determined, which are chosen so that at the cylindrical boundary, $\rho = a$, the tangential components of the field are continuous, i.e.

$$\begin{aligned} &H_z(\rho = +a) = H_z(\rho = -a), \\ &E_\varphi(\rho = +a) = E_\varphi(\rho = -a) \end{aligned} \tag{7}$$

Unknown coefficients can be presented in the form

$$B_k = \frac{\omega\sqrt{\varepsilon_1\varepsilon_2}J_k(k_1a)K_k'\left(\frac{p}{c}a\right) + p\sqrt{\varepsilon_2}J_k'(k_1a)K_k\left(\frac{p}{c}a\right)}{\sqrt{\varepsilon_1}I_k'\left(\frac{p}{v_2}a\right)K_k\left(\frac{p}{c}a\right) - \sqrt{\varepsilon_1\varepsilon_2}K_k'\left(\frac{p}{c}a\right)I_k\left(\frac{p}{v_2}a\right)}U(p),$$

$$C_k = \frac{p\sqrt{\varepsilon_2}J_k'(k_1a)I_k\left(\frac{p}{v_2}a\right) + \omega\sqrt{\varepsilon_1}I_k'\left(\frac{p}{v_2}a\right)J_k(k_1a)}{\sqrt{\varepsilon_1}I_k'\left(\frac{p}{v_2}a\right)K_k\left(\frac{p}{c}a\right) - \sqrt{\varepsilon_1\varepsilon_2}K_k'\left(\frac{p}{c}a\right)I_k\left(\frac{p}{v_2}a\right)}U(p), \tag{8}$$

$$U(p) = \frac{ip(v_2^2 - v_1^2)}{(p - i\omega_0)(p^2 v_1^2 + \omega_0^2 v_2^2)}b_k e^{-pt^*}.$$

The expressions have the poles and the branch-cut along the negative real axis of the complex p-plane. There are poles associated with the frequency of the initial wave $p = i\omega_0$ and the transformed frequency $p = \pm i\, v_2/v_1\, \omega_0$ due to the permittivity changing. There is also an infinite number of poles associated with the zeros of the denominator B_k and C_k in (8). They correspond to the eigenfrequencies of the resonator in its new state.

Using the asymptotic expansions for modified Bessel functions with large arguments, we have

$$pB_k I_k(\frac{p}{v_2}\rho) \to i\frac{v_2^2 - v_1^2}{v_1^2}\frac{c}{c+v_2} b_k \sqrt{\frac{a}{\rho}} J'_k(k_1 a) e^{\frac{p}{v_2}(\rho - a)} \quad (9)$$

$$pC_k K_k(\frac{p}{c}\rho) \to i\frac{v_2^2 - v_1^2}{v_1^2}\frac{c}{c+v_2} b_k \sqrt{\frac{a}{\rho}} J'_k(k_1 a) e^{-\frac{p}{c}(\rho - a)} \quad (10)$$

From (9) and (10) it is observed that, upon inversion to the time domain, the expressions corresponding to $B_k(p)I_k(\rho p/v_2)$ and $C_k(p)K_k(\rho p/c)$ exhibit a time delay that can be expressed in terms of unit-step Heaviside functions, $\Theta(v_2 t + \rho - a)$ and $\Theta(ct - \rho + a)$, inside and outside of the resonator, respectively.

In the "early time" regime ($t < a/v_2$) inside the resonator the field is described by the first term in (5) and exhibits the same wavenumber and shifted frequencies predicted from the abrupt change in the material parameters. It does not depend upon the boundary shape. In the outer region, only the initial field is present. Near the boundary region, the transient waves appear that correspond to total field given in (5) and (6). In the time domain they are expressible in terms of a residue sum over all the singular points and an integral along the branch cut. Examination of (5) and (6) in more detail reveals that the singularities in the total field at $p = \pm i v_2/v_1 \omega_0$ and $p = i\omega_0$ do not contribute to the residue sum. It is also confirmed that there is a term in the transient response inside the resonator that provides immediate cancellation of the primary wave.

In the E polarization case, the problem can be solved in similar way – see [14, 15].

B. Linear chain of resonators

Proposed approach can be extended to a finite linear chain of coupled circular dielectric resonators. We consider the 2D model of the linear chain of N identical circular resonators with the radii a. The separation distance between the resonators is d , the dielectric permittivity of the material is ε_1 . The transversal electric (H-polarized) WGM is considered as an initial field; the z-component of it can be represented in the following form

$$H_z(\rho_j, \varphi_j) = \sum_{s=-\infty}^{+\infty} A_s^{(j)} J_s(k_1 \rho_j) e^{is\varphi_j} \quad \text{inside the } j^{th}$$

resonator,

$$H_z(\rho_j, \varphi_j) = \sum_{j=2}^{N} \sum_{s=-\infty}^{+\infty} \bar{A}_s^{(j)} H_s^{(2)}(k_0 \rho_j) e^{is\varphi_j} \text{ in outer space.}$$

Here (ρ_j, φ_j, z) , $j = 2...N$ is a set of N cylindrical systems of coordinates associated with each resonator, coefficients $A_s^{(j)}$, $\bar{A}_s^{(j)}$ can be found to satisfy corresponding boundary conditions (7) at each boundary as discussed in [16, 17].

At zero moment of time, the dielectric permittivity is changed abruptly in the whole structure from the value ε_1 to the value ε_2 . The field after the medium change satisfies the wave equations (3) written for each particular resonator and surrounding space. We solve this problem similarly to single-resonator case and apply the Laplace transform directly to the wave equations including the initial and boundary conditions at the circular interfaces. Using the addition theorem for the Bessel functions, we arrive at an infinite set of algebraic equations that can be truncated in order to provide a predetermined numerical precision. The resulting field in the time domain is obtained using the inverse Laplace transform.

III. Numerical Results

Here, we introduce dimensionless values: $w_0 = a\omega_0/c$ is the normalized frequency, $T = tc/a$ is the normalized time, $r = \rho/a$ is the normalized distance.

To estimate duration of transient (also called ring-time) period in a single resonator, we plot the time dependence of the field inside the resonator. Here, $WGH_{8,1}$ mode is considered as initial field with $w_0 = 4.5418 + 0.000399i$, and refractive index is $n_1 = \sqrt{\varepsilon_1} = 2.631$. At zero moment of time, the refractive index changes to the value $n_2 = \sqrt{\varepsilon_2} = 2.63$.

Fig. 1 presents the total field normalized by the maximum of amplitude of the initial field versus the normalized time near the centre of the resonator (r=0.05). Changing the refractive index leads to the excitation of all modes with the same angular dependence as initial one however with growing of *r* transient process becomes smooth (Fig. 2). Evaluating the residues at each singular pole, we conclude that maximum amplitude has the mode with the same field pattern as initial one as seen in Fig. 2. The change of the refractive index leads to the frequency shift of the mode from the initial value $\omega_0 = \omega'_0 + i\omega''_0$ to the transformed value $\omega_1 = \omega'_1 + i\omega''_1$.

Fig. 3 represents the absolute value of the normalized frequency shift $\Delta w = \Delta\omega a/c$ ($\Delta\omega = \omega'_1 - \omega'_0$) of the transformed modes with different numbers of angular variations. It is seen that WGM with a greater Q-factor demonstrates a greater frequency shift.

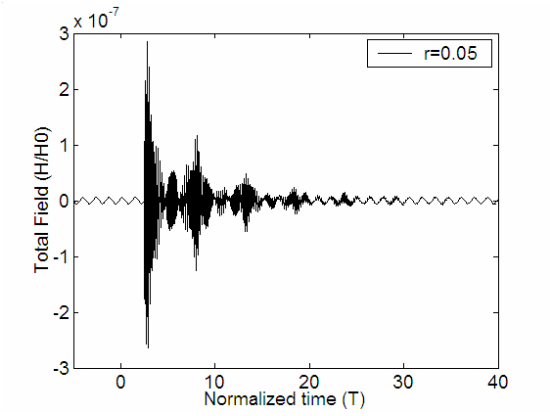

Fig. 1. Time dependence of the transformed field (r=0.05)

Abruptly decreasing the refractive index leads to an increase in the frequency, and increasing the refractive index leads to the opposite effect.

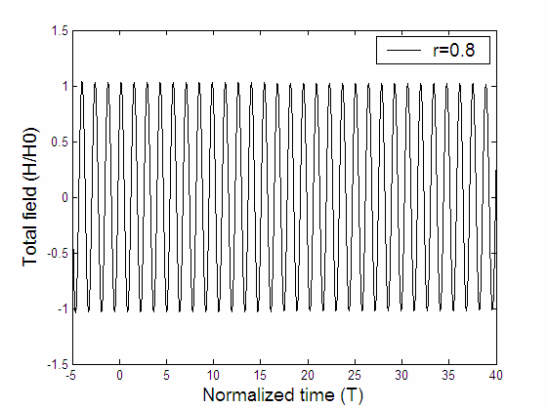

Fig. 2. Time dependence of the transformed field (r=0.8)

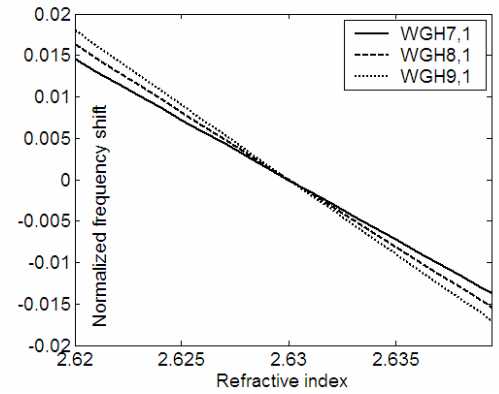

Fig. 3. Normalized frequency shift versus refractive index

Proposed approach has been extended to the case of a linear chain of coupled resonators. If resonators are brought togeter, four families of coupled modes with different types of symmetry with respect to Ox and Oy axes can be excited [10]. Numerical results are presented for two coupled modes with even-even (EE) and odd-odd (OO) symmetry along the Ox and Oy axes. Fig. 4 shows their near field patterns for N=6, with the $WGH_{8,1}$ mode considered as initial field (the same for Fig. 5, 6). Before zero moment of time, $n_1 = 2.63$.

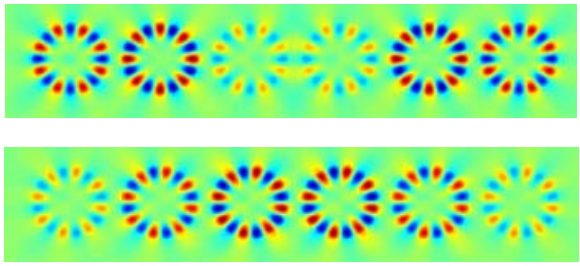

Fig. 4. Near field patterns of EE mode (above) and OO mode (below).

Fig. 5 represents the absolute value of the normalized frequency shift Δw of the transformed mode versus the normalized separation distance between the resonators in the twin resonator structure (N=2). It is seen that for the distant resonator ($d > a$) the frequency shift is the same for the OO and EE modes. The frequency shift decreases for the EE mode and increases for the OO coupled mode if the resonators are brought together.

If the number of resonators in the chain with small air-gaps gets larger, this leads to increase in the frequency shift for the OO coupled mode (Fig. 6).

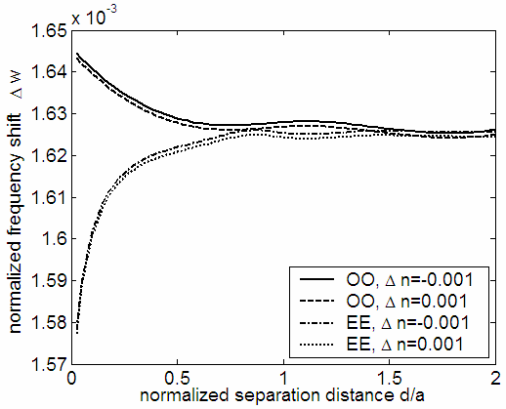

Fig. 5. The normalized frequency shift versus the normalized separation distance between the resonators, N=2

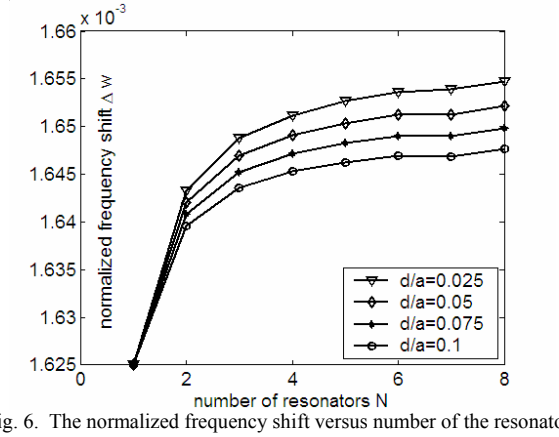

Fig. 6. The normalized frequency shift versus number of the resonators in the chain

VI. Conclusion

In this paper, a theoretical analysis of WGM transformation due to the time variation of the permittivity in a single resonator and in a linear chain of coupled resonators has been developed. The theory is based on eigenfunction expansion in the Laplace transform domain and inversion of the solution into the time domain through the residue evaluation.

The obtained results reveal the resonant frequency shift of the transformed field. Enhancement of the frequency shift for the coupled modes with odd-odd symmetry in the chain has been shown.

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Testing and Diagnosis of Bad Messages in Individual Cyberspace

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Abstract – **The theory, methods and the architecture of parallel information's analysis is presented by the form of analytical, graph and table forms of associative relations for the search, recognition, diagnosis of destructive components and the decision making in n-dimensional vector cybernetic individual space. Vector-logical processes-models of actual oriented tasks are considered. They include the testing and diagnosis of bad massages and the recovery of serviceability, the hardware-software components of computer systems and the decision quality is estimated by the interactions of non-arithmetic metrics of Boolean vectors. The concept of self-development information of computer ecosystem is offered. It repeats the evolution of the functionality of the person. Original processes-models of associative-logical information analysis are represented on the basis of high-speed multiprocessor in n-dimensional vector discrete space.**

I. Introduction

THE problem of creating an effective infrastructure of cyberspace (Cyber Space), as well as self-developing information and computing ecosystems (ICES) of the planet is particularly important for global companies, such as Kaspersky Laboratory, Google and Microsoft.

Cyberspace as an object of nature is also susceptible to destructive components affecting the performance of subjects, which are computers, systems and networks. Therefore, now and in the future it remains as an important problem of space standardization and specialization of all the interacting entities, including the negative, as an integral part of the ecosystem. This action is permanent in time, whose purpose is to keep up, but one step ahead of the emergence of new malicious components, by creating an infrastructure cybernetic space, operating the computer ecosystem of the planet and the quality of each person's life.

Among the modules of such an infrastructure we can provide diagnosis of failures, and spam by analyzing the information obtained at the testing stage and using of special methods of built-in search spam, standard-based boundary scan or assertion redundancy focused on spam detection, it will allow to identify and to eliminate spam without the use of external funds. So, it will be possible to do it without difficult exterior programs of modeling, testing and diagnosing by grafting of each e-mail testability intellectual redundancy package at the stage of its creation. It should use the predicate of recognition, which operates not only Boolean but register and matrix variables, making it nearly significant in formal writing the equations of diagnosis or recognition:

$$x^a \approx x \oplus a = 0 \vee \min_i Q_i \to x \oplus a \oplus Q = 0;$$

$$x^m \approx x \oplus m = 0 \vee \min_i Q_i \to x \oplus m \oplus Q = 0;$$

$$T \oplus S = Q \approx$$

$$\approx \begin{bmatrix} 00 \\ 01 \\ 10 \\ 11 \end{bmatrix} \begin{bmatrix} 1 & . & 1 & 1 \\ . & 1 & . & . \\ . & 1 & . & 1 \\ 1 & . & . & 1 \end{bmatrix} \Delta \begin{bmatrix} 1 & . & 1 & 1 \\ . & 1 & 1 & 1 \\ . & . & . & . \\ . & . & . & 1 \end{bmatrix} = \begin{bmatrix} . & . & . & . \\ . & . & 1 & 1 \\ . & 1 & . & 1 \\ 1 & . & . & . \end{bmatrix}$$

where x^a, x^m – Predicate variables, a, m – values of variables, Q_i – an estimation of a cognizance of variable value; T – the test, S – the object which is subject to testing (program).

On the basis of recognition of the predicate m-image of any complexity, nature and shape can be created quite compact equation predicates forming intellectual solutions in the field of pattern recognition, decision making, testing, knowledge and technical facilities, diagnosis (recognition) among the spam e-mails.

In this regard, the proposed infrastructure of cyberspace, the metric to measure and model the

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process of analysis and synthesis of subjects give the opportunity to create effective solutions for computer products focused on Quick Search, detection and diagnosis not only positive but also negative subjects. Specifically, the proposed infrastructure can solve the problem: 1) Description of the variety of cyberspace e-waste. 2) The formalization of the interaction of triad components <the program, spam, tests>. 3) Diagnosing and e-mail filtration. 4) The creation and effective utilization of spam basis. 5) The creation of high-speed intellectual means of self-developing service and protection of cyberspace.

It laid the basic principles of evolution, expressed even in the modern computer industry: 1) The standardization is the most important thing for evolution and life cycle ICS. The market doesn't accept and doesn't understand non-standard decisions on the interface. 2) Specialization is the efficiency provided by (personally oriented) services, products related to performance, quality, cost, energy saving by optimizing the structure and functional components that cover the specification. 3) Widespread use of vector-logical criteria of quality solutions to the problems of generating ideas, analysis and synthesis. Generation is a process of new functionality creation. In this synthesis it operates with existing components in the information space to create a structure. The analysis is an estimation of the received decision. 4) Hasse diagram is used to develop strategies to optimize coverage of the functional specification of library components or combinations, belonging to the information space. It is consistent with the modern Y-Technology, part of the ESL Design, which uses library components for all levels of product design to meet the Specified functionality in the synthesis process.

Fig. 1 is a vicious cycle of evolution ICES, which is actually isomorphic to the spiral of human development, wound on the time axis.

The purpose of this paper is the significant improvement of the quality of individual cyberspace (ICP) of the user and cost reduction in operating costs due to vaccination ICP by adding a space infrastructure service, which includes libraries of positive and negative messages and provides testing, diagnosis and removal of harmful components of e-mails.

The object of study is a personal cyberspace with the information provided, its carriers and converters, as well as destructive components harmful to the functionality and improves the quality of human life.

Subject of research is the infrastructure service, which includes libraries of positive and negative messages and embedded software redundancy, which operates in real time, provides testing, diagnosis and removal of malicious and "junk" e-mail information, as described in the relevant libraries.

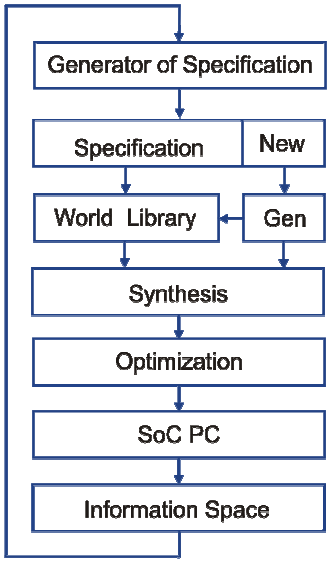


Fig. 1. Cycle ICES

Motivation:

1) Lack of market AntiSpam protection built-in testing, diagnosing and removing harmful components that make up the infrastructure service, just as in digital systems in crystals, there are boundary-scan standards, and software products - assertion redundancy focused on integrated testing of defects and errors, followed by a hardware or software products.

2) The theoretical development related to technology of algebraic vector analysis of information data-oriented high-performance solutions and estimation problems of recognition and images, action and testing facilities.

3) The presence of a model of production and marketing infrastructure of Kaspersky Lab is able to support the project of electronic communication technology vaccination and authority to offer to the market the information technologies.

4) Miniaturization and digital communications systems (phones, smart phones, tablets) require constant protection from the massive and unnecessary e-mails through the introduction of built-AntiSpam means controlling the exchange of information.

Tasks: 1) To develop mathematical tools of analysis of cyberspace based on the creation of models and methods of service of software products for testing, diagnosing and eliminating the massive and unnecessary emails. 2) To create a standard process models and criteria for the interaction of e-mails with content analysis of useful functionality. 3) To develop the technology for analyzing the structure of the program code for determining the critical points and install the assertion operator monitors and manage the process of its functioning. 4) To create the infrastructure service functional programs for the embedded test, diagnosis and removal of harmful components of the software package of functionality through the use of library spam

information. 5) To test and to verify integrated infrastructure service functionality that protects against malicious software code components.

II. Evolution of Cyber Space and Internet

To create a schema that implements useful functionality, it should generate the lowest level primitives. You must create filters $F = \{F_1, F_2, ..., F_j, ..., F_m\}$ that form a table of primitive relations, taken from the informational space of the planet (Fig. 2). Having a standardized data structure for the individual portals and browsers, delivering new services with higher speed you should expect a gradual qualitative improvement of all components of Cyber Space. The ultimate goal of such a mutual and positive impact of the infrastructure of cyberspace is to develop uniform standards for the interfaces and its transformation into a self-developing intelligent information computer ecosystem. Significant importance will be the primary filters or converters to create the new standardized primitives, creating a technological infrastructure for high-speed drive on the Cyber Space with the use of specialized non-arithmetic engine (I-Computer). With time, the amorphous or "garbage" of the Internet will decrease and standardized infrastructure grow. By 2020, the informational space of the planet must adopt civilized formats of data structures with standardized interfaces, just as it has happened with the development of a planetary infrastructure, transport connections to the terminals, hotels and gas stations, satisfying all user requests.

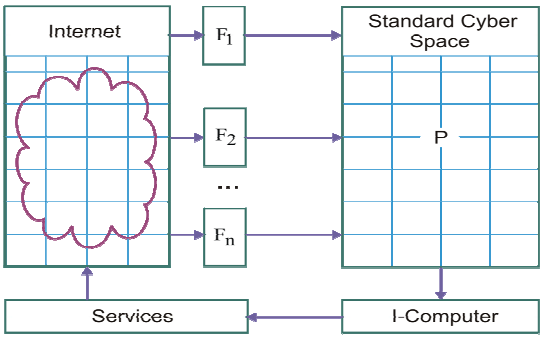


Fig. 2. The Evolution of Cyber Space and the Internet

With a specification provided after processing a verbal description in the form of a vector of input and output variables, it is easy to write a strategy to build a new functionality as the task of finding covered by the library elements of the generalized vector <X,Y>. The general solution of the problem is similar to the synthesis of an automaton model that defines the interaction of components in time and space. However, a variety of primitives are not specified in advance, excludes such a possibility, which means a shift from the strict determinism of digital machines to the field of evolutionary and quasi-solutions.

The condition of the problem: there is a specification as a vector of the essential variables that needs to cover a minimal set of primitives from the library and to generate an output vector. A beautiful solution to the problem of the functional structure synthesis of the specification is the key to self generating computer for new solutions. After the solution is solved only two problems are left on the way to the creation of computer intelligence – itself-generate original functionality required to solve the problem of coverage and specifications of new and useful for human or computer services.

III. Integral Metric Evaluation of the Diagnosis

Infrastructure brain-like algorithms for detecting spam includes models, methods and associative logical data structure intended to support the search process, to recognize and to make decisions based on non-arithmetic vector operations. The score is determined by solving the problem of vector-logical criterion of quality interaction between the query (a vector m) with a system of associative vectors (associates) which will generate a constructive response in the form of one or more associates and the numerical characteristics of the power supplies (quality function) input of vector m to found solution: $\mu(m \in A)$. The input vector $m = (m_1, m_2, ..., m_i, ..., m_q)$, $m_i \in \{0,1,x\}$ and a matrix A_i of associators

$$A_{ijr}(\in A_{ij} \in A_i \in A) = \{0,1,x\}$$

have an identical dimensionality equal q. Further the accessory level of m-vector to A vector will be designated as $\mu(m \in A)$.

There are 5 types set-theoretic (logical) Δ-interactions of two vectors $m \cap A$ defined in fig. 3.

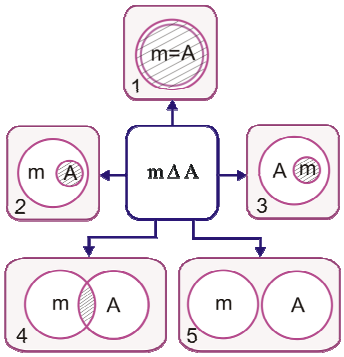


Fig. 3. The results of the intersection of two vectors

They form all primitive choices of generalized PRP-SYSTEM response (Search, Recognition and Decision

making) to an input vector request. In the technology industry knowledge technical diagnostics (Design & Test) is a specified sequence of actions, it is isomorphic to the itinerary: the search for defects, their detection, the decision to restore health. All three stages of a technological route need the evaluation metric solution for the optimal choice.

Definition. Integral theoretical metric for evaluating the quality of the query is a function of the interaction of multi-valued vectors $m \cap A$, which is determined by the average sum of three normalized parameters: the minimum distance $d(m, A)$, the membership function $\mu(m \in A)$ and membership function $\mu(A \in m)$:

$$
\begin{aligned}
&Q = \frac{1}{3}[d(m, A) + \mu(m \in A) + \mu(A \in m)],\\
&d(m, A) = \frac{1}{n}[n - \mathrm{card}(m_i \bigcap_{i=1}^{n} A_i = \varnothing)];\\
&\mu(m \in A) = 2^{\mathrm{card}(m \cap A) - \mathrm{card}(A)} \leftarrow \mathrm{card}(m \cap A) =\\
&= \mathrm{card}(m_i \bigcap_{i=1}^{n} A_i = x) \,\&\, \mathrm{card}(A) = \mathrm{card}(\bigcup_{i=1}^{n} A_i = x);\\
&\mu(A \in m) = 2^{\mathrm{card}(m \cap A) - \mathrm{card}(m)} \leftarrow \mathrm{card}(m \cap A) =\\
&= \mathrm{card}(m_i \bigcap_{i=1}^{n} A_i = x) \,\&\, \mathrm{card}(m) = \mathrm{card}(\bigcup_{i=1}^{n} m_i = x).
\end{aligned}
\tag{1}
$$

Explanations. Valuation parameters allow to evaluate the level of interaction vectors in the interval [0,1]. If we set limiting maximum value of each parameter equal to 1 then the vectors are equal. Minimum score $Q = 0$ records in the case of a complete mismatch of the vectors for all n coordinates. If the power of intersections $m \cap A = m$ is equal to half of the space vector A, the membership function and quality are equal:

$$
\mu(m \in A) = \frac{1}{2};\ \mu(A \in m) = 1;\ d(m, A) = 1;
$$

$$
Q(m, A) = \frac{5}{2 \times 3} = \frac{5}{6}.
$$

A similar value would be setting if the power of intersections is equal to half of the space of the vector m. If the power of intersections is equal to half of the capacity of the spaces of vectors and m, the membership functions have values:

$$
\mu(m \in A) = \frac{1}{2};\ \mu(A \in m) = \frac{1}{2};\ d(m, A) = 1;
$$

$$
Q(m, A) = \frac{4}{2 \times 3} = \frac{4}{6} = \frac{2}{3}.
$$

It should be noted if the intersection of two vectors is equal to empty set, the power of two characters from "empty" is taken to be zero:

$$
2^{\mathrm{card}(m \cap A) = \varnothing} = 2^{\varnothing} = 0.
$$

It really means that the number of common points at the intersection of two spaces is zero.

The aim of introducing vector logical criteria of the solution quality is significantly improved by the performance in calculating the quality Q of interaction between the components m and A in the analysis of associative data structures by using only the vector logic operations. Arithmetic criteria (1) without averaging membership functions and minimum distance can be transformed to the form of:

$$
\begin{aligned}
&Q = d[m, A_{i(j)}] + \mu[m \in A_{i(j)}] + \mu[A_{i(j)} \in m],\\
&d(m, A_{i(j)}) = \mathrm{card}[m \underset{i(j)=1}{\overset{n(m)}{\oplus}} A_{i(j)} = 1];\\
&\mu(m \in A_{i(j)}) = \mathrm{card}[A_{i(j)} = 1] - \mathrm{card}[m \underset{i(j)=1}{\overset{n(m)}{\wedge}} A_{i(j)} = 1];\\
&\mu(A_{i(j)} \in m) = \mathrm{card}[m = 1] - \mathrm{card}[m \underset{i(j)=1}{\overset{n(m)}{\wedge}} A_{i(j)} = 1].
\end{aligned}
\tag{2}
$$

The first component creates the degree of mismatching n-dimensional vectors, it is the minimum distance by performing xor, the second and the third ones determines the degree of non-membership result of the conjunction to the number of units of each two interacting vectors. Notions of belonging and not-belonging are complementary but in this case it is better to calculate technological nonaffiliation. Thus, the ideal quality criteria are zero when two vectors are equal. The assessment of interaction quality between two binary vectors decreases with increasing test from 0 to 1. Finally to get away from arithmetic when you count a vector quality criteria help the expression (2) transformed to:

$$
\begin{aligned}
&Q = d(m, A) \vee \mu(m \in A) \vee \mu(A \in m),\\
&d(m, A) = m \oplus A;\\
&\mu(m \in A) = A \wedge \overline{m \wedge A};\\
&\mu(A \in m) = m \wedge \overline{m \wedge A}.
\end{aligned}
\tag{3}
$$

Here the criteria are not numbers and vectors, which evaluate the interaction of components. The increase in the number of zeros in the three vectors improves the quality criterion and the availability of units indicates the deterioration of the interaction quality.

IV. Process Model of Diagnosing SPAM

Quality metric presented in (3) makes it possible to assess the proximity of spatial objects to each other as well as the interaction of the vector spaces. A practical example of the usefulness of integral quality criteria may be shooting at the goal which is illustrated by the

previously reduced diagram (see Fig. 3) of the interaction vectors:

1) The shell hit the target and did it completely. 2) The target was struck by unreasonably large caliber projectile. 3) Caliber projectile is insufficient to defeat a major purpose. 4) Inefficient and inaccurate shot by large caliber projectile. 5) The projectile flew past the target.

Process-interaction model is accompanied by integral quality criteria which evaluates not only hit or miss but also the caliber efficiency of the weapon. The analytical form of a generalized process model that selects the best interaction between the input query m to the system logic associative relationships are represented as follows:

$$P(m,A) = \min Q_i(m \overset{n}{\underset{i=1}{\Delta}} A_i) =$$

$$= \vee[(Q_i \overset{j\neq i}{\underset{j=1,n}{\wedge}} Q_j) \oplus Q_i] = 0;$$

$$Q(m,A) = (Q_1, Q_2, ..., Q_i, ..., Q_n);$$

$$A = (A_1, A_2, ..., A_i, ..., A_n);$$

$$\Delta = \{and, or, xor, not, slc, nop\};$$

$$A_i = (A_{i1}, A_{i2}, ..., A_{ij}, ..., A_{is});$$

$$A_{ij} = (A_{ij1}, A_{ij2}, ..., A_{ijr}, ..., A_{msq});$$

$$m = (m_1, m_2, ..., m_r, ..., m_q).$$

$$Q_i = d(m, A_i) \vee \mu(m \in A_i) \vee \mu(A_i \in m), \quad (5)$$

$$d(m, A_i) = m \oplus A_i;$$

$$\mu(m \in A_i) = A_i \wedge \overline{m \wedge A_i};$$

$$\mu(A_i \in m) = m \wedge \overline{m \wedge A_i}.$$

In order to detail the structure of vector calculations the analytical and structural process models are presented below which are given for the analysis of A matrix by columns or lines.

The proposed process model analysis (graph) of associative tables identified by the components of spam and introduced by the quality criteria for logical decisions that allow us to solve the problem of quasi-optimal coverage, diagnosing varieties of spam messages in an individual cyberspace (ICP) users. The model of vector calculations has provided the basis for the development of specialized multiprocessor oriented architecture search, pattern recognition and decision making when using the associative structure of tables (Fig. 4).

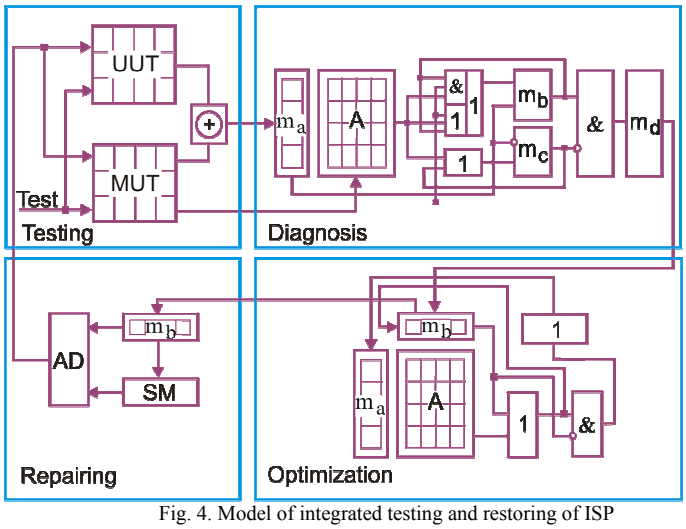


Fig. 4. Model of integrated testing and restoring of ISP

The evaluation of effectiveness (Fig. 5) of the design solution under the auspices of specialization and standardization $S_p \cup S_t$ is based on the combined use of three mutually conflicting parameters: the quality Y, speed T, the program costs H:

$$E = F(Y, T, H),$$
$$Y = (1-P)^{n(1-Q)};$$
$$T = \frac{1}{f} \times S \times d;$$
$$H = 2(H^s \times n).$$

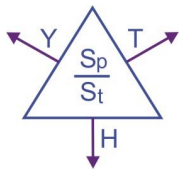


Fig. 5. Evaluation of the effectiveness of the process model

V. Practical Results of the Implementation of Infrastructure

As an object of investigation was chosen SquirrelMail - email client with a Web interface written in PHP. The application can be installed virtually on any web server that has PHP installed and there is a connection to the mail server for IMAP and SMTP. The interface window is shown in Fig. 6.

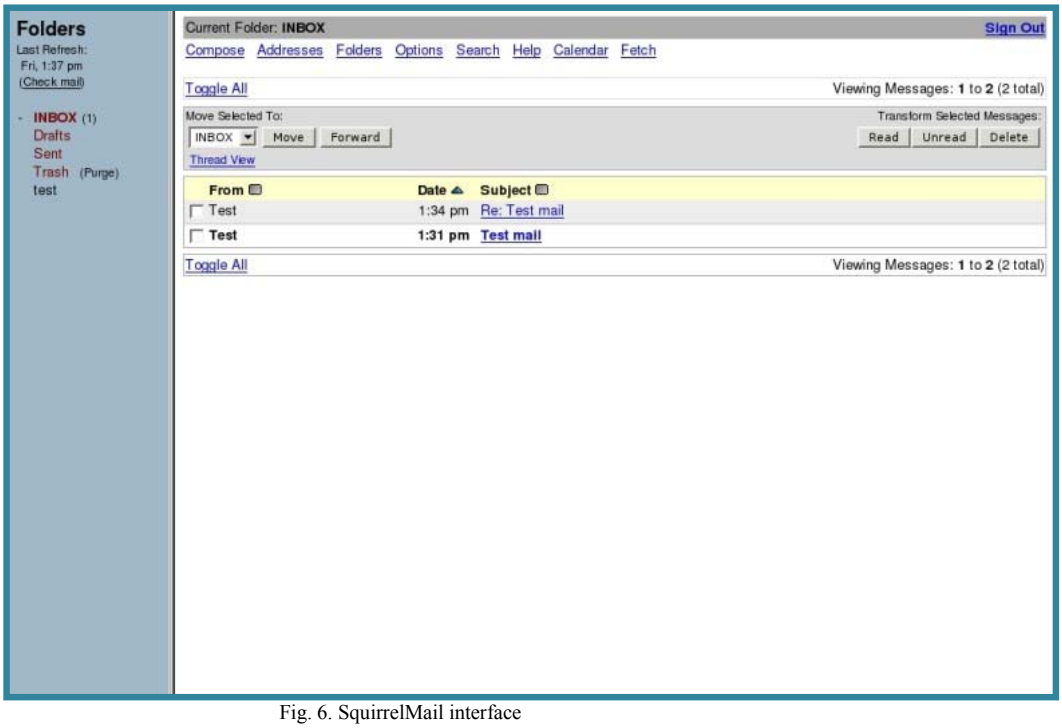


Fig. 6. SquirrelMail interface

This client is easily expanding by different plugins. To conduct the study was written a plugin that implements the analysis of determination of usefulness of information based on user preferences. The process-model of the plugin is shown in Fig. 7. Based on the user's activity and the attributes of content analysis of the letter, the filter system was selected and studied. While downloading new messages from an individual cyberspace (in this case cyberspace was presented by a subset of e-mails), the information was filtered not on the "spam"or "not spam" basis but on the basis of personal preferences of the user (Fig. 8).

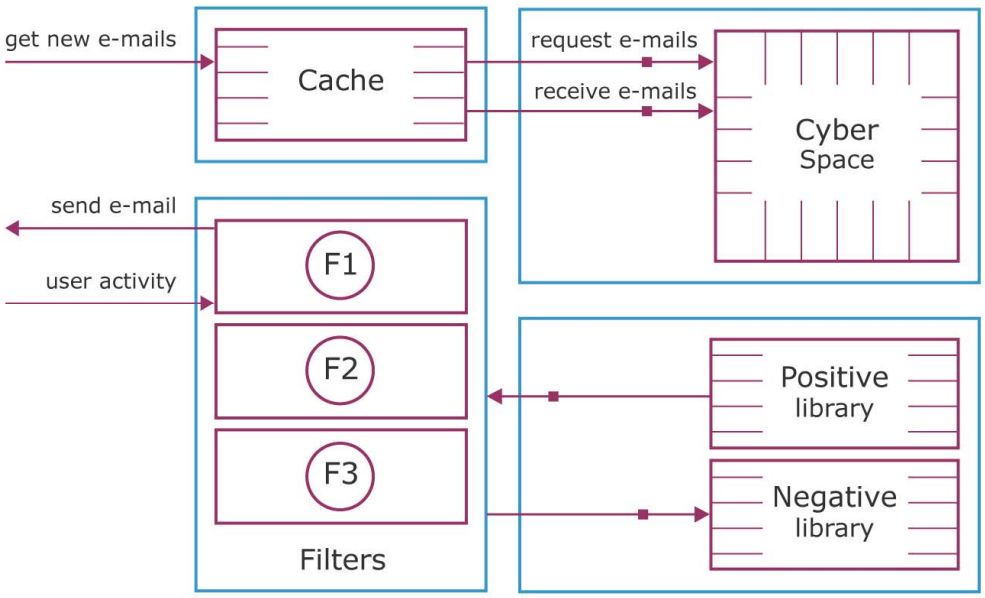


Fig. 7. The process-model of the plugin for SquirrelMail

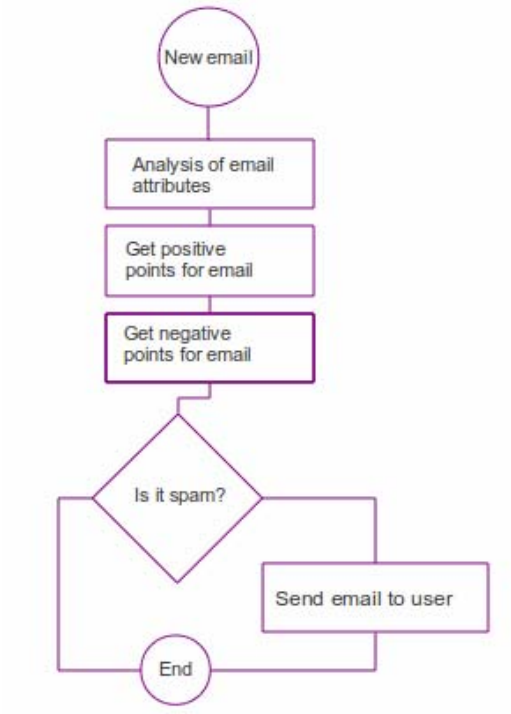
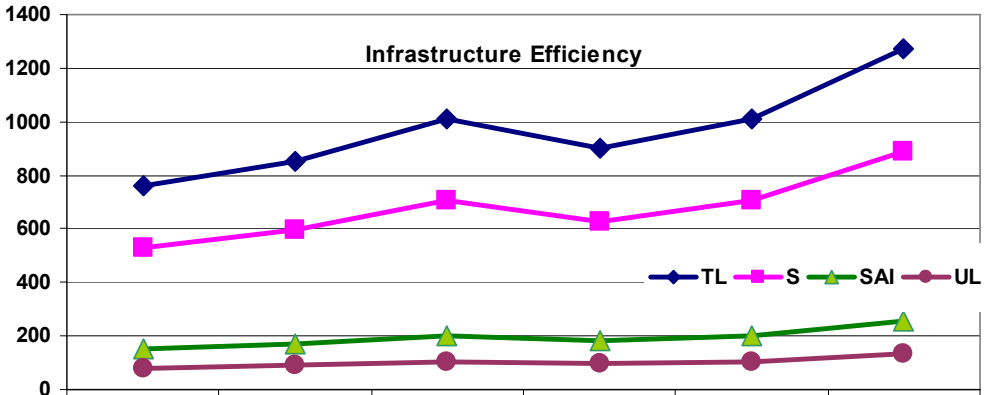


Fig. 8. Graph-scheme of the letter analysis

From the entire set of letters arriving at the mailbox, "spam" (anonymous mass mailings) has been partially identified not as a spam, but as distribution, which can carry out useful information for the user. Fig. 9 shows the effectiveness of introducing of the infrastructure service ICS for a single user, where the TL - Total Letters, S - Spam, SAI - Spam after Infrastructure, UL - Useful Letters. If we assume that the market attractiveness of the infrastructure is around the order of 1 billion users, the time savings in the overall market of cyberspace users is (T_{Σ} – total time savings per year ; k - the reducing ratio of spam in the implementation of infrastructure; L - the number of letters per month; N - the potential number of users in Ukraine; T - time analysis of a single letter; M - number of months per year; H_{Σ} – the annual financial savings from the introduction of infrastructure; C_h – the cost of one hour of work of a single user in Ukraine)

$$T_{\Sigma} = k \times L \times N \times T \times M = 0{,}9 \times 800 \times 100000000 \times 1 \times 12 = 864000000000c \approx 2740 years \approx 24002400 hours;$$

$$H_{\Sigma} = T_{\Sigma} \times C_h = 24002400 \times \$5 = \$120012000$$



	Jul	Aug	Sept	Oct	Nov	Dec
TL	760	850	1010	900	1010	1270
S	532	595	707	630	707	889
SAI	152	170	202	180	202	254
UL	80	89	106	95	106	133

Fig. 9. The effectiveness of implementation of ICS infrastructure

VI. Conclusion

1. *Scientific novelty* of the study results is that the servicing infrastructure of individual cyberspace was proposed for the first time and characterized by the presence of built-in testing, diagnosing and restoring of the ICS and two growing library of positive and negative messages, which gives the opportunity to significantly (by several times) reduce the analyzing time of received information.

2. *The practical* significance of the research results of infrastructure ICS service was focuses on the quality improving of life for all stakeholders of the planet that are using email services to communicate with the outside world. In this case ICS is a model of the future of human communication with the outside world, which is invariant with respect to the technical means available in the cyberspace world. The annual economic effect from the introduction of the ICP infrastructure for Ukrainian users can make more than $ 120 million.

3. *The direction of future researches.* Urgent problem is the creation of the theory, methods and architecture of the parallel analysis of information provided in the form of analysis, graph and tabular forms of associative relations for search, recognition, diagnosis and destructive components of decision making in the n-dimensional vector discrete space. It is advisable to use here a vector-logical process model of topical applications, including a diagnosis of viruses and disaster recovery software and hardware components of computer systems, the quality solutions of which are estimated by nonarithmetic metric interaction of binary vectors. Solving the problem is focused on search, detection, diagnosis of the destructive components of hardware and software by methods in discrete cyberspace. Generality of the provided theory of synthesis and analysis of cyberspace is based on the vanishing of the triad of equivalent components that are connected by xor $m \oplus A \oplus Q = 0$ operation, formulating the conditions for solving the problem. Here, the first component m is the input code, the second A - is a destructive reference model, third Q – is the result of interaction between the first two, which may degenerate into criteria of quality relationships or decision making, the assessment of recognition of objects or images.

The goal is a substantial improvement of the quality of software products and cost reduction in operating costs due to their vaccination by introducing a code embedded software redundancy in the form of infrastructure service that provides testing, diagnosis and removal of harmful classified in libraries. The object of study is cyberspace presented by information, its carriers and converters as well as destructive components harmful to the functionality that improves the quality of human life. The subject is infrastructure of service in the form of built in redundancy program running in real time, which provides testing, diagnosis and removal of harmful components, described in the relevant libraries.

4. *Expected results and its market appeal:* 1) infrastructure protection of built in code from unauthorized modification, leading to a change in functionality. 2) The redundancy of infrastructure code that is automatically synthesized at the stage of design and verification is not more than 5% of the specified functionality. 3) The market attractiveness of infrastructure with the variety of software products, multiplied by the sales of each product that is equal to about one billion copies per year. 4) The cost of creating an infrastructure for software is 20% of the cost of developing functional code. If the level of sale is not less then 500 copies, the costs of creating a completely integrated antivirus payback within a year. 5) The introduction of patented software of vaccination products at their birth can bring to the company about 2 billion dollars in the first 3 years of its operation. 6) The marketing problem of global companies (Kaspersky Lab) is in persuading software developers to implement existing antivirus inside the code of useful functionality.

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Research and Development Solution Methodology of Informative Features Choosing for the RES Life Cycle Processes Analysis

Nevlyudov I.Sh., Andrusevich A.A., Khatnyuk I.S.

Abstract — **The methods of solving the problem of choosing the informative features to identify the RES functioning are offered by classifying the RES and life cycle processes in the feature space, and each of which has a value that allowed us to find a comprehensive criterion and formalize the selection process.**

I. Introduction

The functional problem of selecting informative features for monitoring the life cycle of radio electronic systems (RESs LC) can be solved within the framework of development methodology for dictionary attributes in the classification systems and the objects state identification [1-5]. In the working vocabulary one should use only those features that, on the one hand, are the most informative and that, on the other hand, may be available for measurement.

The description of the dictionary of features under conditions of constraints on the cost of observation hardware creation has some particulars. If the objects attributes are denoted by δ_j, j=1, 2,…, N, each object in the N-dimensional space of attributes can be represented as a vector $x = (x_1, x_2, ..., x_N)$, its coordinates characterize the properties of objects.

To determine the measure of closeness or similarity between objects in N-dimensional attributes vector space a metric is introduced. The Euclidean metric can be used as

$$d^2(w_{pk}, w_{ql}) = \sum_{j=1}^{N} (x^j_{pk} - x_{ql}{}^j)^2, \qquad (1)$$

$p, q = 1, 2, ..., m; \quad k = 1, 2, ..., k_p; \quad l = 1, 2, ..., k_q,$

where $p, q = 1, 2, ..., m; \quad k = 1, 2, ..., k_p; \quad l = 1, 2, ..., k_q,$

x^j_{pk} are the values of j-feature, k is an object, p is a class, i.e. the q is an object class, i.e. object w_{ql}.

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As a measure of proximity between the objects of this class Ω_p, $p = 1, 2, ..., m$, we will use the value

$$S(\Omega_p) = \sqrt{\frac{2}{k_p} \frac{1}{k_{p-1}} \sum_{k=1}^{k_p} \sum_{l=1}^{k_p} d^2(w_{pk}, w_{pl})}, \qquad (2)$$

that makes sense as class rms dispersion or the rms scatter of objects within class Ω_p, as a measure of proximity between a given pair of objects of classes Ω_p and Ω_q, $p, q = 1, ..., m$, is the value

$$R(\Omega_p, \Omega_q) = \sqrt{\frac{1}{k_p k_q} \sum_{k=1}^{k_p} \sum_{l=1}^{k_q} d^2(w_{pk}, w_{ql})}, \qquad (3)$$

that makes sense of rms dispersion of a class of objects Ω_p and Ω_q.

A set of objects features that are used in the working vocabulary can be described as an N-dimensional vector $A = (\alpha_1, \alpha_2, ..., \alpha_N)$, whose components takes the values 1 or 0 depending on whether there is or is not a possibility to determine the appropriate object feature.

Taking into account the *a* is the squared distance between two objects w_{pk} and w_{ql} the unequation given below will take the form

$$d^2(w_{pk}, w_{ql}) = \sum_{j=1}^{N} \alpha_j (x^{(j)}{}_{pk} - x^{(j)}{}_{ql})^2. \qquad (4)$$

Consequently, the rms scatter of the class Ω_p and objects of classes Ω_p and Ω_q can be written as

$$S(\Omega_p) = \sqrt{\frac{2}{k_p} \frac{1}{k_p - 1} \sum_{k=1}^{k_p} \sum_{l=1}^{k_p} \sum_{j=1}^{N} \alpha_j (x^{(j)}{}_{pk} - x^{(j)}{}_{pl})^2}, \qquad (5)$$

$$R(\Omega_p, \Omega_q) = \sqrt{\frac{1}{k_p} \frac{1}{k_q} \sum_{k=1}^{k_p} \sum_{l=1}^{k_q} \sum_{j=1}^{N} \alpha_j (x^{(j)}{}_{pk} - x^{(j)}{}_{pl})^2}. \qquad (6)$$

One can take into consideration that the cost of using the feature is proportional to the information contained in them, i.e. to such quantities of objects features that can be determined with their help. This assumption is fairly general.

Thus, the cost of using the features amount to

$$C = C(\alpha_1, ..., \alpha_N) = \sum_{j=1}^{N} C_j \alpha_j, \qquad (7)$$

where C_j is costs to determine the j-sign.

As an indicator of quality or effectiveness of the designed recognition system we consider the functional, which depends in general on the function $S(\Omega_p)$, $R(\Omega_p,\Omega_p)$ and decision rule $L(w,\{w_g\})$

$$I = F[S(\Omega_p);\ R(\Omega_p,\Omega_q);\ L(w,\{w_g\})]. \quad (8)$$

Let the value $L(w,\{w_g\})$ be a measure of proximity between the recognizable object w and class Ω_g, $g = 1, 2, ..., m$, that is given by its objects $\{w_g\}$. As this measure of proximity let's consider the value

$$L(w,\{w_g\}) = \sqrt{\frac{1}{k_g}\sum_{g=1}^{k_g} d^2(w,w_g)}, \quad (9)$$

which is mean square distance between the object w and the classes objects Ω_p.

The decision rule consists in the following

$$w \in \Omega_g, \text{ если } L(w,\{w_g\}) = \text{extr } L(w,\{w_i\}). \quad (10)$$

It is important to note that the decrease in $S(\Omega_p)$, "compression" of objects belonging to a given class, while increasing $R(\Omega_p,\Omega_q)$, i.e. "division" of objects belonging to different classes improve the quality of the recognition system. Therefore, improving the efficiency of the system will be linked to the achievement of functional extremum I.

II. Formulation of research problems

Formulation of research problems can be represented as follows.

Let the entire set of objects be divided into classes Ω_i, $i = 1, ..., m$, a priori all classes being described in the language of features x_j, $j = 1, ..., N$, and funds, whose value is equal to C_0, are allocated for creating observation hardware. It is required that a working vocabulary of features be built which provides the maximum possible efficiency of the system without exceeding the allocated funds.

Thus, the problem reduces to finding the condition extremum of the functional which looks like (8), i.e. to the definition of A which implements the

$$\underset{\alpha}{\text{extr}}\ I = \underset{\alpha}{\text{extr}}\ F\ [S(\Omega_p);\ R(\Omega_p,\Omega_q);\ L(w,\{w_g\})]$$

$$C = \sum_{j=1}^{N} C_j \alpha_j \le C_0. \quad (11)$$

Consider some special types of the functional (11). If the required efficiency of the recognition system can be achieved through a more compact arrangement of objects in each class, subject to certain conditions regarding the magnitude of $R(\Omega_p,\Omega_q)$, then the problem reduces to finding

$$\min_{\alpha}\ \max_{i=1,...,m}\ [S(\Omega_i)] \quad (12)$$

when

$$\sum_{j=1}^{N} C_j \alpha_j \le C_0 \ \text{ и } \ R(\Omega_p,\Omega_q) \ge R_0^{(pq)}. \quad (13)$$

If the required system performance can be achieved through the "bias" objects that belong to different classes under certain conditions with respect to the value $S(\Omega_i)$, $i = 1, \ldots, m$, then the problem reduces to finding

$$\max_{\alpha}\ \min_{p,q=1,...,m}\ [R(\Omega_p,\Omega_q)] \quad (14)$$

when

$$\sum_{j=1}^{N} C_j \alpha_j \le C_0 \ \text{ и } \ S(\Omega_i) \le S_0^i. \quad (15)$$

If a proper system performance can be achieved only by increasing the ratio of distances between the classes to the rms scatter within the classes of objects, then the problem reduces to finding

$$\max_{\alpha}\ \min_{p,q=1,...,m}\left[\frac{R^2(\Omega_p\ \Omega_q)}{S(\Omega_p)S(\Omega_q)}\right] \quad (16)$$

when

$$\sum_{j=1}^{N} C_j \alpha_j \le C_0. \quad (17)$$

III. The selection problem solution of informative features that characterize the state of the RES LC processes

The problem considered above is a generalization of a nonlinear programming problem. Optimality conditions for it can be formulated as follows: in order the vector C^0 to be an optimal strategy, it is necessary that there exist a scalar $\beta \ge 0$ and vector $\mu = \{\mu_1, ..., \mu_n\}$ which will be equal

$$\left.\begin{array}{l} \left[\sum_{r=1}^{n} \mu_r \rho_r^j\right] \dfrac{dP_j(C_j^0)}{dC_j} = \beta, \quad j = 1, ..., N_p; \\ \sum_{j=1}^{N_p} C_j^0 = C_0\ ; \\ \sum_{r=1}^{n} \mu_r = 1,\ \mu_r = 0, \quad \text{если} \quad \sum_{j=1}^{N_p} \rho_r^j P_j(C_j^0) > W(C^0). \end{array}\right\} \quad (18)$$

An introduction to the consideration of scalar β and vector μ increases the number of unknowns C_j^0, μ_r and β to a value $N_p + n + 1$. However, the number of equations equals the number of unknowns, since for every r or $\mu_r = 0$, or

$$\sum_{j=1}^{N_p} \rho_r^j P_j(C^0{}_j) = W(C^0). \quad (19)$$

Thus, the solution of the system (18) makes it possible to determine the composition of the working vocabulary signs and optimal allocation of costs to provide tools for observing the recognition system under the assumption of depend-

ence of $P_j = P_j(C_j)$ and limitations to the total cost of these funds.

With the limitations associated with the ability to use a dictionary of all attributes, the problem arises of choosing a limited list (up to 2-3 characters). Here it is possible navigate in the location of the individual components of feature vector with respect to the boundaries of performance facilities monitoring.

Since for the boundary value of the parameter y^j_{rp}, the end of the vector X must be located on the boundary of operability, it is necessary to satisfy the equality

$$x^i{}_{rp} = a^i_j y^j{}_{rp}. \qquad (20)$$

A correlation coefficient r_{ij} between the parameters may be an additional criterion for selection under statistical estimation. Since the maximum correlation coefficient provides a maximum amount of information

$$J(y^j) = H(y^i) - H(y^j / y^i), \qquad (21)$$

contained in the parameter y^i. Here $H(y^i)$ is the initial entropy; $H(y^j / y^i)$ is the conditional entropy of the object after the measurement of parameter y^j.

The use of a binary correlation algorithm allows for the participation of decision makers (DM) to formalize and automate the processes of input, processing, and recognition of an image.

IV. RES LIFE CYCLE PROCESSES STATE IDENTIFICATION

The solution of the RES life cycle identification, involves creation the rules that define the RES state.

The signs, that allow to distinguish the state of an object under monitoring, are efficiency indicators, which will have a given value or an extreme value for the selected state. To identify the RES state from the observed parameters in the monitoring process it is necessary to select a set of parameters, in which the value of performance indicators will have given or extreme values.

The objects of observation - the parameters and characteristics of RES - can be considered as points of vector and functional spaces. For all pairs of points in the set Q, there is a binary relation of the comparative effectiveness: point x is more efficient than point y then and only then when (x,y) ϵ Φ or in another writing x ϵ y. The problem of allocating the core is solved by ensuring the RES life cycle – a set of maximal elements of the variables X to a binary relation $\Phi : X^* = \mathrm{Max}\ (Q, \Phi)$.It is assumed that the solution of the problem exists i.e. set X* is not empty. In many problems, we may assume that the solution is a set X* which consists of one element, and the relationship between the elements is established by means of functionals $\Lambda(x)$. For instance, the point x is more effective than point y, when $\Lambda(x) < \Lambda(y)$ or $\Lambda(x) > \Lambda(y)$. It can be shown that in problems of determining the effective pixels $x_0 \in X^*$ with constraints $x \in Q_1$, the functional $f = \lambda\Lambda'(x_0)$, where Frechet derivative $\Lambda'(x_0)$ at the point x_0 is support functional to Q_1, at the point x_0 (i.e. $(f, x_0) < (f, x)$ for all $x \in Q_1$.

Thus, the problem of analyzing the results of observations in the monitoring process is reduced to the determination of support functionals at points of observation, which makes it possible to estimate the deviation of the observed points from effective points.

In terms of functional analysis [4,5]: let Q be some set in linear topological space E, E' be the dual space, $x_0 \in Q$ is an extreme point of Q, K_b is the cone of possible directions in Q at the point x_0, K_k is the cone of tangent directions for Q in x_0. If the set of linear functionals, which are reference to the Q at the point x_0, denotes the Q*, then Q*=$\{ f \in E', f(x) \ge f(x_0)$ for all $x \in Q$, i.e. support functional and the extreme point $x_0 \in Q$ provide an opportunity to allocate a set Q. It can be shown that if Q is closed convex set, then $Q^* = K_k{}^*$, i.e. forms a cone formed by the set of linear functionals reference to Q in x_0. The cone of tangent directions can be determined from the Frechet derivatives of the operators (convex function), which connect the sets of parameters and performance indicators.

Let us consider the methods of finding K* for ways to specify K using different functionals.

Example 1. In the case of determination Q using affine sets: $E = E_1 \times E_2$; E_1, E_2 are the linear topological space, a performance characteristics set is defined E_2, D is a linear operator from E_1 to E_2, $K = \{x \in E, x = (x_1, x_2) : Dx_1 = x_2\}$, $K^* = \{f \in E', f = (f_1, f_2) : f_1 = -D^* f_2\}$, and as a reference separating function one can use the expression

$$f(x) = (-D^* f_2, x_1) + (f_2, x_2) = -(f_2, D^* x_1 - x_2).$$

Application of this function to separate the sets in the parameter space and the formulation of rules, that establish a correspondence between the sets of parameters and values of performance indicators, can provide the identification of states in the process of monitoring RES LC.

Example 2. A functional $\Lambda(x)$ in the linear space E has a derivative $\Lambda'(x_0, g)$ at the point x_0 in the direction of g, there is

$$\lim_{\varepsilon \to +0} \frac{\Lambda(x_0 + \varepsilon h) - \Lambda(x_0)}{\varepsilon} = f(x_{0,} g). \qquad (22)$$

The functionals are correctly decreasing at any point and allow us to find the cone of decreasing directions. The func-

tional $\Lambda(x)$, which is a set in a Banach space E, is differentiable (or Frechet differentiable) at x_0, if there exists a linear functional $f \in E'$ such that for all $g \in E$

$$\Lambda(x_0 + g) = \Lambda(x_0) + (f, g) + o(\|g\|). \quad (23)$$

If $\Lambda(x)$ is differentiable at the point x_0, then $F(x)$ is correctly decreases at the point x_0 and $K = \{g : (\Lambda'(x_0), g) < 0\}$. K is decreasing direction cone of the functional $\Lambda(x)$ at the point x_0, $\Lambda(x)$ (satisfies a Lipschitz condition in a neighborhood of $x_0 \in E$, $\Lambda(x)$ is differentiable at x_0 in any direction, and $f(x_0, g)$ as a function of g is convex if $g \in K$ and $\Lambda'(x_0, g)\ g \in E$, E is a Banach space, $\Lambda(x)$ satisfies a Lipschitz condition in the neighborhood of x_0 (for some $\varepsilon_0 > 0$ $|\Lambda(x_1) - \Lambda(x_2)| \le \beta\|x_1 - x_2\|$ for all $\|x_1 - x_0\| \le \varepsilon_0$, $\|x_2 - x_0\| \le \varepsilon_0$) and $\Lambda'(x_0, g) < 0$ will be satisfied, then $\Lambda(x)$ is correctly decreasing at x_0, and $K = \{g : \Lambda'(x_0, g) < 0\}$.

Example 3. In the case of the set, which is not defined by a functional. If Q is a convex set, then the decreasing direction set K_b at x_0 takes the form

$$K_b = \{\lambda(Q^0 - x_0), \lambda > 0\}$$

(i.e. $K_b = \{g : g = \lambda(x - x_0),\ x \in Q^0, \lambda > 0\}$).

Example 4. $P(x)$ is an operator from E_1 in E_2, that is differentiable in a neighborhood of x_0, $P(x_0) = 0$. $P'(x)$ is continuous in the neighborhood of x_0, and $P'(x_0)$ displays E_1 for all E_2 (i.e. linear equation $P'(x_0)g = b$ has a solution g for every $b \in E_2$), then the set of tangent directions K to set $Q = \{x : P(x) = 0\}$ at x_0 is the subspace $K = \{g : P'(x_0)g = 0\}$.

When the $P'(x_0)E_1 \ne E_2$, one can only state that $K \subset \{g : P'(x_0)g = 0\}$.

Example 5. Let $x \in R^m$, $Q = \{x : G_i(x) = 0,\ i = 1, ..., n\}$, where $G_i(x)$ are functions continuously differentiable in a neighborhood of x_0, $G_i(x_0) = 0$, $i = 1,...,n$, and vectors $G_i'(x_0)$, are linearly independent. Then $K = \{g \in R^n : (G_i'(x_0), g) = 0, i = 1,..., n\}$.

Here $E_1 = R^m$, $E_2 = R^n$, $P(x) = (C_1(x), ..., G_n(x))$, $P'(x_0)$ is matrix $m \times n$, i column is equal to $G_i'(x_0)$.

Example 6. In the process of monitoring it is necessary to determine whether the effective value of the function- RES characteristics $w(z)$ is provided and if in the simplest case the extreme value of an differentiable objective function is provided for one variable, for which it is necessary to check whether the derivative is zero at the observed value of the parameter. For multi-dimensional objective functions and their arguments, this problem may be conceded as part of set theory and functional analysis.

Formalizing in the observation problem of optimal setting, as one of the RES life cycle processes, lies in the fact that it is necessary to estimate optimal function of the process setting $v(z) \in M$, where z is the parameter determining the numerical value of the required characteristic $w(z)$ of a setting object to provide such a phase trajectory, which ensures the equality $w(0) = c$, $w(Z) = d$ and extreme values of the integral functional $\int_0^Z \Phi(w(z), v(z), z)dz$, in the case of a connection, given by the differential equation $\frac{dw(z)}{dz} = \varphi(w(z), v(z), z)$.

In problems that requires maximum compliance of an optimised characteristic to some desired characteristic, minimum mean square deviation criterion is used

$$W_2(X) = \overline{(Y(X) - Y^*)^2}, \quad (24)$$

where Y^* is the value characteristic desired or required by the technical project.

For the characteristic, which is given by a discrete set of points, the objective function

$$W_2(X) = \frac{1}{N}\sum_{i=1}^{N} \gamma_i (Y(X, p_i) - Y_i^*)^2, \quad (25)$$

where N is the number of sampling points of the independent variable p; $Y(X,p_i)$ is the value of the optimized performance in the i-th point of the sampling interval; γ_i – optimized characteristic weight coefficient values that reflects the importance of the i-th point compared with other points (usually, $0 < \gamma_i > 1$).

In some optimization problems it is necessary to ensure the excess or not the excess of some given level optimized characteristics. These criteria of optimality are implemented by the following functions:

– to provide excess of a given level

$$W_3(X) = \begin{cases} 0 & \text{at } Y(X) \ge Y_H^*, \\ (Y - Y(X))^2 & \text{at } Y(X) < Y_H^*; \end{cases} \quad (26)$$

– to provide unexcess of a specified level

$$W_4(X) = \begin{cases} 0 & \text{at } Y(X) \le Y_B^*, \\ (Y(X) - Y_B^*)^2 & \text{at } Y(X) > Y_B^*, \end{cases} \quad (27)$$

where Y_H^*, Y_B^* are the feasible region lower and upper bounds for the characterization of Y(X).

If it is necessary that an optimized characteristic be within some permissible zone (boundary), a combination of two previous optimization criteria are used

$$W(X) = \begin{cases} 0 & \text{at } Y_H^* \le Y(X) \le Y_B^*, \\ (Y(X) - Y_B^*)^2 & \text{at } Y(X) > Y_B^*, \\ (Y_H^* - Y(X))^2 & \text{at } Y(X) < Y_H^*. \end{cases} \quad (28)$$

For those cases when it is necessary to implement only the shape of the curve while ignoring a constant vertical bias, there the shift criterion is used.

$$W_6(X) = \sum_{i=1}^{N} \gamma_i (Y_i^* - Y(X, p_i) - Y_{cp})^2, \quad (29)$$

where $Y_{cp} = \frac{1}{N} \sum_{i=1}^{N} (Y_i^* - Y(X, p_i))$.

The form of objective function effects the computing process important characteristics and, convergence of the optimization process. Derivatives signs of the objective function for the controlled parameters are not constant throughout the feasible area, this circumstance leads to the ravine of the character (for example, problems of circuit design), which leads to high computing cost and requires special attention to the choice of optimization method.

Another feature of the objective functions is that they usually multiextremal and along with the global minimum have local minima.

A general class of problems identifying the set of efficient solutions consists of multi-criteria optimization problems. They are characterized by the fact, that binary relation on the set of alternatives is associated with a set of indicators, forming an efficiency vector criterion. This binary relation is generated by a variety of ways. Thus, if the

$$W(x) = (W^1(x), ..., W^m(x)) \quad (30)$$

is vector criterion on the set of X, than binary relation can be Pareto ratio, or ratio of Slater. In other cases, a binary relation on X is defined by a system of preferences of the decision maker (DM). It is assumed that the main source of information is a person who has information sufficient to make a (unique) solution. Identification of the system of DM preferences represents one of the main problems in solving multiobjective problems. Usually a procedure for identifying the decision maker preferences are based on the language of vector evaluations of alternatives.

Algorithms based on scalarization – reducing to a parametric family of scalar optimization problems – are most illustrative.

IV. Conclusion

The scientific result of the paper is as follows: methods of informative features selection were developed that solve the problems for monitoring the RES life cycle, by classifying the states of RES and the life cycle processes in the feature space, each of them having a particular significance. This has allowed to find comprehensive criteria and formalize the selection process. Heuristic methods for selecting the criteria for the use of prototypes and basic information priorities are proposed, when there is an insufficient number of a priori data for correct classification.

The methods of solving the problem of choosing informative features of RES LC processes were researched that will allow a meaningful description of the processes for implementing RES LC decision-making procedures in the man-machine systems.

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The Essentials of Testing Digital Circuits

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Abstract – Testing is an important part of digital devices development life cycle and it takes about 70% of time to market. This paper discusses the various testing concepts as it relates to digital design and how it impacts the reliability of the final product. We also show that making designs testable by using appropriate design for testability techniques considerably reduces testing time and ensures a fine-grained diagnosis of finished product. A three bit counter circuit was used to illustrate the benefits of design for testability by using scan chain methodology.

Index Terms – Reliability, design for testability, faults, defect level.

I. Introduction

The reliability of electronic system used to be the concern of the military, aerospace and banking industries. But today applications such as computers, consumer electronics, telecommunication and automotive industries have joined the league of applications that demands reliability and testing techniques because they are everywhere and their feature sizes have become less and less as the years go by. In addition, their proliferation has led to the tendency of their misuse. An important aspect of reliability is the system's ability to run independently on demand. This requires that the system be fault tolerant.

Poor quality products require more maintenance and repairs which leads to huge expenses on staff and mileage to get staff and spares to outdoor locations [4]. It also affects the manufacturer's image and costs on returned parts and systems.

The three basic engineering activities are design, manufacture and test. Currently testing activities are also carried out at the design stage. This means that testing process is integral to both design and manufacturing activities and cannot be seen as a standalone activity. These activities are done as quick as possible and economically too. Because we want to save time and cost, we should endeavour to ensure that the quality of the would-be product is not compromised. Even while a product is in use testing can also be carried out either as a normal routine service arrangement or to eliminate faults as they occur.

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A good quality product must meet the purpose for which it was designed and produced. In addition it must be very reliable meaning that the device should be operational most of the times and rarely fails. The reliability of Digital devices is high. But this reliability can be undermined if the operational conditions are not adhered to. Conditions such as operating temperature, power supply voltages and frequencies, electromagnetic influences and handling can negatively affect the reliability of digital devices. If the room temperature is higher or lower than the recommended for example, the device may over heat and probably damage some of the components which may render the device inoperable.

If we can guarantee 98% fault free circuit at the design and implementation stages, we may not be able to say what happens after packaging and when the component is finally mounted on a board and delivered to the consumer. It is important to note that ICs at the end of the day find there ways onto a circuit board. Even Systems on chip (SoC) end up on a board. While on the board we have to boarder about how well the pins of the various ICs mounted on the board are connected or whether the right IC is in the right position.

Testing encompasses design verification and diagnosis (fault location for purposes of effecting repairs). There are two aspects to test. One is testing the design, or carrying out design verification to make sure the design is correct and conforms to requirements. Design verification also lets you know where you are in the development cycle and how stable the design is [1]. The other aspect of test is testing for physical failures, making sure nothing is been broken and there's no defect from manufacturing. A significant portion of our development cycle time is spent on testing the product design, and that's becoming extremely expensive.

The beauty of integrated design and manufacturing is that it cuts product cycle time, but successful integration hinges on the quality of the design data passed to manufacturing. This paper focuses on the fundamentals of testing at the design stage. The remaining parts of this paper were divided into sections. In section 2 the challenges of product quality will be discussed. Section 3 briefly discusses the design flows with integrated testing. In section 4, this paper reviews faults and test pattern generation, whereas section 5 x-rays ways of making designs testable. A simple example to illustrate the design for testability technique using scan chain methodology was presented in section 6.

II. Testing Challenges

Quality improvement starts at the design stages. Testing starts right from the system level through RTL coding to

fabrication and use of the device in the field. Currently assertions are embedded in codes to help for quick localisation of functional violations during simulation. It is a standard in electronics industry to test chips before they are mounted on a board, test the board before system assembly and finally test the system. This is essentially so because of the rule of ten. If a chip fault is not caught by chip testing, finding the fault costs 10 times as much at the PCB level as at the chip level. Similarly if a board fault is not caught by PCB testing, finding the fault costs 10 times as much at the system level as at the board level. This means that a fault that is not caught at the chip level will now cost 100 times as much at the system level.

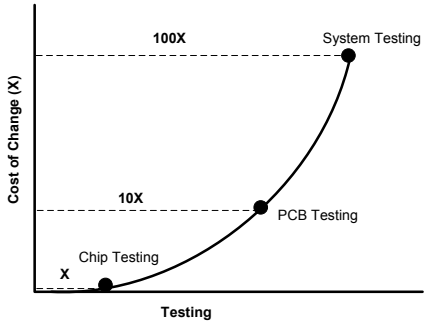

Fig. 1. The Rule of Ten

Some engineers are suggesting that rule of twenty be adopted considering the complex nature of present day ICs. The rule of ten is illustrated in figure 1. Very real costs are associated with inattention to design quality. If errors or omissions in design data are not addressed early, more costly changes are required later in the product development process.

Another development is the synthesis for different objectives. Early synthesis was aimed at decreasing area and delay. More recently, other objectives have come into play, such as power, noise, thermal control, verifiability, manufacturability, variability, and reliability. Consequently, additional criteria will emerge as new technologies develop, and new models and optimization techniques will be needed to address such requirements [12].

Concept of reliability

Reliability is the probability of no failure within a given operating period. For example, if 50 systems operate for 1,000 hours on test and two fail, then we would say the probability of failure, P_f , for this system in 1,000 hours of operation is 2/ 50 or P_f (1,000) c 0.04. Clearly the probability of success, P_s, which is known as the reliability, R, is given by $R(1,000)=P_s(1,000) =1-P_f (1,000)=48/50= 0.96$.

One can also deal with a failure rate, f_r, for the same system that, in the simplest case, would be $f_r = 2$ *failures/ (50 × 1,000)* operating hours — that is, $f_r = 4 \times 10^{-5}$ or, as it is sometimes stated, $f_r=z=40$ failures per million operating hours, where z is often called the hazard function. If failure rate z is a constant (one generally uses λ to represent a constant failure rate), the reliability function can be shown as in (1).

$$R(t) = e^{-\lambda t} \quad (1)$$

The mean time between failures (MTBF):

$$MBTF = \int_0^{\infty} e^{-\lambda t} dt = \frac{1}{\lambda} \quad (2)$$

The repair time (Rep) is also assumed to obey an exponential distribution and is given by.

$$\text{Re}\, p(P > t) = e^{-\mu t}. \quad (3)$$

The mean time to repair (MTTR):

$$MTTR = \frac{1}{\mu}, \quad (4)$$

Where, μ is the repair rate. The system availability (failure-free) is the fraction of time the system is operating normally and is given by:

$$\text{System Availability} = \frac{MTBF}{MTBF + MTTR} \quad (5)$$

With the above expression for reliability it becomes evident that the more complex a system is the less is its reliability. For instance if a system board contains n number of components and each component has a reliability of R_c, the reliability of the board (R_{sb}) over time t period of operation without failure is:

$$R_{sb} = [R_c(t)]^n = [e^{-\lambda t}]^n = e^{-n\lambda t} \quad (6)$$

It is therefore clear that the system reliability is very small not minding the fact that the reliability of individual component is high and will reduce further if the reliability of the interconnections were taken into consideration.

The graphical representation of failure rate Z(t) as a function of time can be illustrated by the popular bathtub curve shown in figure 2.

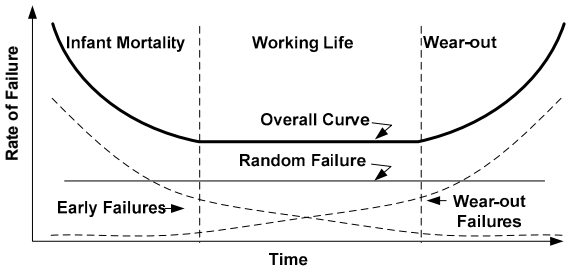

Fig. 2 Failure rate curve

The infant mortality region on the graph depicts failures that are attributed to poor quality as a result of variations in the production process technology. The region on the graph termed "Working life" shows that the failure rate is constant *(Z(t)=λ).* This is the working life of the component or system and fault occurrence here is at random. The wear out region marks the end-of-life period of a product. For electronic products it is assumed that this period is less important because they will not enter this region due to a shorter economic lifetime as a result of technology advances and obsolescence. It is important to note here that all ICs

must be shipped after they have passed infant mortality test periods in order to reduce field failure and subsequent repairs.

III. Design Flows

The design of VLSI follows certain procedure, evolving from the highest level of abstraction down to implementation - Design Specification, HDL Capture, RTL Simulation & Functional Verification, RTL Synthesis, Functional Gate Simulation, Place and Route and Post Layout Timing Simulation.

Every design starts with specification capture. We must determine the functionality of the new design at the onset. Wrong conception at this level could lead to a lot of problems such as poor quality product or overlooked functionality. An idea of what is to be designed is converted into formal document called design specification. In some cases one or more specification documents are created, depending on whether we are creating a component or a system. Design specification is a written statement of functionality, timing, area, power, testability, fault coverage, etc. The following methods are used to specify the functionality – state transition graphs, timing charts, algorithmic state machines and hardware description languages (VHDL and Verilog). Lately the need to capture designs at the highest level of abstraction in what is called Electronic System Level (ESL) using SystemC, System Verilog, etc. is being integrated and pursued vigorously. The specification is then captured using HDL in form of behavioural description. The HDL model of the design is simulated in order to determine functional compliance and to expose any design or coding errors. In order to achieve this, a test plan is developed. This involves writing a test bench for the model and applying appropriate test vectors to verify the design. If the functionality has been verified, then the model is synthesised using appropriate synthesis tools. The objective of synthesis is to produce a netlist (list of modules and their interconnection at the register transfer level stage or at the gate level) of the design for the target technology. Synthesising the design involves optimisation of Boolean functions (minimise logic, reduce area, reduce delay, reduce power, balance speed versus other resources consumed). After the RTL/gate level synthesis, the design is further simulated to determine that the gates used functions properly and meets the overall functionality. If this is achieved then we move on to the placement and routing stage where selected cells are placed on the target technology (CPLD, FPGA or ASIC) and connected in accordance with the netlist. After the placement and routing have been completed the need to further simulate the design arises. In this case we simulate to determine whether the timing (timing back-annotation), speed, physical and electrical specifications have been met. This simulation includes test vector generation to test for inherent fabrication flaws. It is important to note that the design should be correct at this stage, because this is the last stage before the design is signed off for fabrication. You can see that testing is carried out virtually at all of the stages of the design flow. This is important because the earlier an error is detected the better and of course the cheaper.

Verification and Testing occur at different levels of product development. Design verification is a set of activities that is carried out on a circuit before the circuit is implemented physically. These activities are geared toward ensuring that the circuit under design meets its functional and timing specifications. Mapping a design from one phase to another may cause some errors to occur. These errors may be as a result of improper handling of the EDA tools and they must be removed before the next phase. You see that at each stage the design is verified to assert that it is the same design from the previous stage and that it meets the specification. Currently simulation is the most efficient method of design verification. We simulate for functional and timing compliance. Assertion-based verification is gradually gaining in popularity amongst design and verification engineers.

Testing on the other hand is a set of activities designed to ensure that a circuit that has been manufactured complies with the parametric (voltage, resistance, current, capacitance, etc), timing and functional specifications of the design. In other words testing demonstrates that the manufactured IC is error free. Digital testing is performed on the manufactured IC using test patterns that are generated to demonstrate that the product is fault-free. It is important to note that at the logic gate level automatic test pattern generation (ATPG) is used to generate the test patterns and are verified using fault simulators. At higher levels of abstraction (RTL and behavioural) testability measures are used instead.

Rapidly evolving submicron technology and design automation has enabled the design of electronic systems with millions of gates integrated on a single silicon die, capable of delivering gigaflops of computational power. At the same time, increasing complexity and time to market pressures are forcing designers to adopt design methodologies with shorter ASIC design cycles. With the emergence of system-on-chip (SoC) concept, traditional design and test methodologies are hitting the wall of complexity and capacity. Conventional design flows are unable to handle large designs made up of different types of blocks such as customized blocks, pre-designed cores, embedded arrays, and random logic. A key requirement for obtaining reliable electronic systems is the ability to determine that the systems are error-free [6]. Electronic systems consist of Hardware and Software. In this paper we shall be looking at hardware testability issues. What is a system? Semiconductor components are not thought of as systems. A system is a collection of components that forms a complete item that one can procure to do a specific task or function. A system also includes a hierarchy of other systems, which we call subsystems, each of which is a system in its own right. In [1] Hal Carter opined that the basic philosophy is that systems grow as large as our technology will permit and testing complexity also grows. If you take n units and combine them such that they all interact, you'll get $n(n-1)/2$ interconnections, which is a

n^2 product of the communication complexity between the units. If you can decompose that, you can get down to $\log n$ complexity for the number of units actually being diagnosed or tested. Design-for-test and self-test must therefore be involved with components at as many levels as possible. Then system-level testing can actually aggregate those lower level tests in a more streamlined way as they migrate towards the system as a whole [1].

IV. Review of Faults And Test Pattern Generation

With the present deep sub-micron technology which is currently at 20nm [7] ensuring high product reliability has become more daunting. The more transistors/gates we squeeze into a small area of a chip the greater the risk of over heating, crosstalk between interconnections and the more likely the chip is subjected to failure. This has not been the case because of the enormous effort the design and verification engineers spent in testing the would-be IC. The would-be chip is subjected to rigorous testing to expose any fault in terms of functional compliance and power violations. Apart from design errors, faults also result from manufacturing process. Testing continues right after the IC is mounted on a board – system test.

A. Fault types and fault models

A digital circuit whose implementation is different from its intended design is said to be defective. And if the output of the circuit is wrong because of the defect we say an error is observed. When we talk about defects from a higher level of abstraction in terms of circuit function, we refer to them as faults. One is talking about the imperfections in the hardware whereas error refers to the imperfections in the functionality of the hardware. An IC may become faulty not only as a result of incorrect design or manufacturing procedure but also as a result of external influence (electromagnetic influence), mechanical rupture, wear and tear. Hard failures (permanent failures) are usually caused by breaks due to mechanical rupture or incorrect design/manufacturing procedure. Soft failures are transient or intermittent. These are induced by supply fluctuations or radiation. Intermittent failures are caused by the degradation of component parameters.

Faults play a great role in helping test engineers detect defects in ICs. In another word we can say that faults are models that help us to understand physical defects. A fault model is a representation of the effects of defects on chip behaviours. A fault model may be described at logic, circuit, or physical levels of abstraction. Examples of fault models include stuck-at faults, bridging faults, stuck-open faults, and path delay faults [13]. Several defects can be mapped to a single fault model. Some defects may also be represented by more than one fault model. In view of the fact that faults are models, they may not really be a perfect representation of the defects, but are useful for detecting the defects. There are so many fault models for representing defects at behavioural, functional or structural levels. The most commonly used fault model at the structural level is single stuck at fault (SSA). This is a situation whereby a line in a circuit is permanently at logic 1 or 0 levels. So we say that a line has a fault stuck-at-1 or stuck-at-0. Though SSA fault has been used widely for defects representation, it has become increasingly imperative to use other models especially with the current complexity of digital circuits. Examples of SSA include a short between ground (s-a-0) or voltage (s-a-1) and a signal; an open on a unidirectional signal line; any internal fault in the component driving its output that it keeps a constant value.

B. Fault Simulation

Fault simulation consists of simulating a circuit in the presence of faults. Comparing the fault simulation results with those of the fault-free simulation of the same circuit simulated with the same applied test, we can determine the faults detected by that test. Faults are simulated in order to achieve the following:

- To evaluate the quality of a test set (i.e. to compute its fault coverage.
- Reduce the time of test pattern generation. A pattern usually detects multiple faults and fault simulation is used to compute the faults accidentally detected by a particular pattern.
- To generate fault dictionary. This is necessary for post test diagnosis.
- To analyze the reliability of a circuit.

C. An example of fault detection and test pattern Generation

In order to illustrate how SSA fault model can be used to detect defects and possibly use the patterns to locate them we shall use a simple 2-input XOR gate figure 3. Table 1 shows the function of an XOR gate under various conditions. Column 2 of the table shows the normal response for fault free nodes, whereas columns 3 upwards show faulty responses of the gate under faulty conditions. A fault is said to have occurred when the circuit's normal response is different from the faulty response for the same set of input combinations i.e. $F \neq F_f$ .This can also be expressed as follows: $F \oplus F_f = 1$.

With the above expression in mind and a closer look at the table indicates that faults are not always observable. For instance, with lines A/0 for input combinations 00 and 01, $F = F_f$. The only time the fault free response differs from the faulty response was when the input combinations AB=10 and AB=11 were applied on the circuit. These input combinations can be considered as the test pattern that detects line A stuck-at-0. Because the two patterns detect

A/0 either AB=10 or AB=11 can be chosen as the test pattern. Let us now consider faults that are detected by specific input combinations.

AB=	00	detects	A/1, B/1 and F/1
	01	detects	A/1, B/0 and F/0
	10	detects	A/0, B/1 and F/0
	11	detects	A/0, B/0 and F/1

From the above we can see that the same input combination detects more than one fault. The first test pattern from the above is AB=00 which covers faults A/1, B/1 and F/1. The next pattern is 01 which detects A/1, B/0 and F/0. With these two patterns we have detected five faults namely A/1, B/0, B/1, F/0 and F/1. We are left with one fault i.e. A/0 to be detected. Any of the patterns AB=10 or AB=11 detects this fault. The set of test vectors that will detect all SSA faults for a 2-input XOR gate are: 00, 01 and 11. This means that if want to test a 2-input XOR fig. 3.2 gate it is sufficient to apply all three of these patterns on the inputs of the gate. The fault coverage in this case is 100%. It is important to observe that this example is a trivial one indeed and oversimplification of testing and test pattern generation procedure.

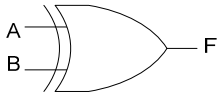

Fig. 3 2-input XOR Gate

TABLE I
XOR GATE RESPONSES UNDER VARIOUS CONDITIONS

Inputs	Fault Free Response	Faulty Response					
A B	F	A/0	B/0	F/0	A/1	B/1	F/1
					F_f		
0 0	0	0	0	0	1	1	1
0 1	1	1	0	0	0	1	1
1 0	1	0	1	0	1	0	1
1 1	0	1	1	0	0	0	1

In practice it is a more daunting task as we have to deal with circuits with millions of gates and different interconnection structures. For example, if we have a tester that is capable of applying test pattern every 100ns, then we can calculate the test time as shown in table 2.

TABLE 2
EXHAUSTIVE TESTING TIME

No. of Inputs	No of tests required for exhaustive testing	Test time
10	2^{10}	102 μSec
20	2^{20}	0.1 Sec
40	2^{40}	30.5 Hours
60	2^{60}	3656 Years

The computational complexity of exhaustive testing is in the order of 2^n. It can be seen in table 2 that the number of tests quickly gets out of hand as the number of inputs increases and therefore it is only of use where there are a very small number of inputs. This testing strategy is also very inefficient since most of the test patterns are actually redundant.

Test pattern generation for sequential circuits is very tedious and less straightforward than for combinational circuits. There are many techniques for test pattern generation, but their discussion is beyond the scope of this paper.

D. Test quality components

Fault coverage (7) is a measure employed generally to determine the quality of tests. It is expressed as a ratio of faults detected (covered) by the test pattern to the total number of faults possible for the given fault model. Because of the difficulty in testing ICs exhaustively some of the faulty ones may escape detection leading to yield and defect level problems. Process yield (8) is a fraction of the manufactured ICs that is defect-free. The process yield is approximated by the ratio of the good ICs to the total number of ICs. Process variations, such as impurities in wafer material and chemicals, dust particles on masks or in the projection system, mask misalignment; incorrect temperature control, etc. affect the process yield. It suffices to note that testing cannot improve process yield. However, process diagnosis and correction can improve process yield. This method involves the location of defects in the failed parts and tracing them to specific causes, which may be defective material, faulty machines, incorrect human procedures, etc. Once the cause is eliminated, the yield improves.

When some of the faults escape detection for some components or parts the defect level increases. Defect level (9) is the fraction of faulty chips among the chips that pass the test, expressed as parts per million (*ppm.*). A defect level of 100 PPM or lower represents high quality. This means that among the so-called good parts or ICs there are bad ones. It is well known fact that the quality is a function of user's satisfaction. To a user the highest quality product is one that meets requirements at the lowest possible cost. Testing (functional) checks to ensure that final product conforms to its requirements and the reduction of cost is achieved by enhancing the process yield. The relationships between fault coverage (FC), yield (Y) and defect level (DL) are as shown in the expressions below:

$$FC = m/n \tag{7}$$

$$Y = (1-p)^n \tag{8}$$

$$DL = 1 - Y^{(1-FC)} \tag{9}$$

Where: n is the total number of faults, m is the number of detected faults $m \le n$, p is the probability of any fault occurring.

The following assumptions were made.

1. Stuck-at-fault model is assumed,
2. The probability (p) of any fault occurring is independent of the occurrence of any other fault. That is to say that the faults are mutually exclusive.

For more detailed information on how they were derived please refer to page 15 of [11]. With 100% fault coverage as

in the example 4.3 the defect level is 0, meaning that none of the components that passed the test is defective. If the coverage is less than 100% it then means that some faults may still exist.

V. MAKING DESIGNS TESTABLE

Testing is an expensive activity in terms of generating the test vectors and their application to the digital circuit under test. Because of the complexity of testing processes, design for testability (DTF) approaches was developed. The DTF approach is aimed at making digital circuits more easily testable such that these circuits are more controllable and observable by embedding test constructs into the design. There is no formal definition for testability. An interesting attempt was given in [9] as: "A digital IC is testable if test patterns can be generated, applied, and evaluated in such a way as to satisfy predefined levels of performance (e.g., detection, location, application) within a predefined cost budget and time scale". One of the key words is "cost." It is probably the cost of testing that deters semiconductor manufacturers from doing as much testing as is really needed to ensure reliable products [10].

There are many facets to this cost, such as the cost of:

1. Test pattern generation (automatic and/or manual) time. Test pattern generation is an NP-complete problem since it is difficult to find a polynomial solution.
2. Fault simulations and generation of fault location information,
3. Test equipment (Automatic Test Equipment).
4. Test application which includes the process of accessing appropriate circuit lines, pads or pins, followed by application of test vectors and comparison of the captured responses with those expected; time required for detecting and/or isolating a fault.
5. Undetectable faults; unpredictable production schedules and an uncertain level of product quality delivered to the customer. When many actual faults are not detected by the derived tests, it is often reflected in terms of loss of customers.

The cost associated with undetected fault could be high, see figure 1, but sometimes difficult to quantify. Although this fault is difficult to quantify, it influences the other costs by imposing high fault coverage requirement to ensure that fault escape is kept below an acceptable threshold [11].

In view of the fact that these costs can be exorbitant and in most cases exceed design costs, it is therefore, necessary to keep them within acceptable limit. And this is the reason why design for testability has become imperative. It is a proven way of reducing testing costs. A fault is testable if there is a well-specified procedure to expose it, which can be implemented with a reasonable cost using current technologies. And a circuit is testable with respect to a fault set when each and every fault in this set is testable. As there is price for everything in this world, DFT carries its own penalty - silicon real estate and performance penalties. This is mainly because of the extra circuitry employed for implementing the DFT.

Testability, on the other hand, is introduced at the design stage, where it dramatically lowers the cost of test and the time spent at test. Properly managed, testability heightens your assurance of product quality and smoothes production scheduling.

A. DFT at the Design stage

Modern design approach has brought test engineering closer to the design activities in that the test program development for an electronic circuit occurs at an early stage in the product development process and requires a basis in design. This overcomes the problems encountered when design and test activities were separate and distinct, an unnecessary barrier between two interrelated activities. In this DFT approach, test activities can influence how a design is created by identifying testability issues and improving test access to specific circuitry within the design. Specialist engineers in both design and testing are supported by a generalist DFT engineer, shown in Figure 4 who bridges the gap between them. The need for specialists is based on the need for in-depth knowledge of specific design and test issues, roles which a single person could not realistically be expected to undertake. [5]

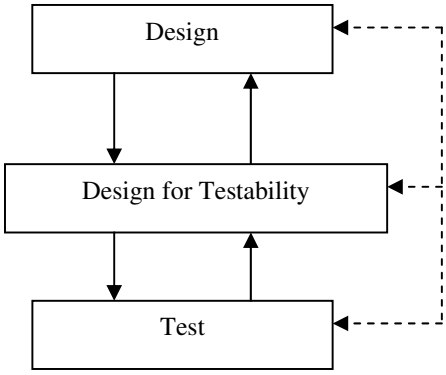

Fig. 4. Integrated designs for testability

B. DFT Methodology

There are several methods of making designs testable. None of these methodologies can solve all VLSI testing problems nor can a single technique guarantee effectiveness of testing for all kinds of circuits. Generally DFT techniques have the capability to increase the circuit real estate on chip which results in complexity of logic circuits. Increased complexity leads to increase in power consumption and decrease in yield. With all these challenges in mind, there is need to select a technique for a particular kind of circuit that balances these trade-offs (benefits and challenges). If a circuit is modified to increase its testability by the addition of extra circuitry, it therefore means that another mode of operation apart from the normal mode has been included. This new mode of operation is called test mode. In this mode the circuit is configured for testing alone. DFT methods include the following: Ad-hoc methods; Scan, full and partial; Boundary scan; Built-In Self-Test (BIST).

The goal of DFT is to increase controllability, observability and/or predictability of a circuit. The DFT

discipline started with the ad-hoc technique which involves the insertion of test points, counters/shift registers, partitioning of large circuits, logical redundancy and breaking of global feedback paths. Many of these ad-hoc techniques were developed for printed circuit boards and some are applicable to IC design. These methods referred to as ad hoc (rather than algorithmic) because they do not deal with a total design methodology that ensures ease of test generation, and they can be used at the designer's option where applicable. The detailed description of these techniques can be found in [8].

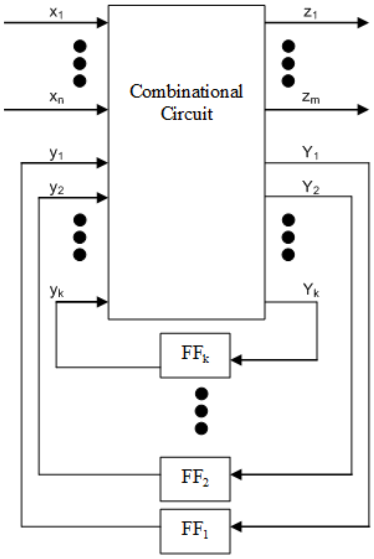

Fig. 5. General Model of FSM

Scan path is a scheme that facilitates the testing of finite state machines (sequential circuits). Automatic test pattern generation for sequential circuits is very tedious and in most cases do not achieve the required test coverage. This arduous task is as a result of the difficulty in controlling and observing the inputs and output states of the flip flops respectively. In this technique the flip flops (FF) or latches are designed and structured in such a way that allows the circuit to be operated in either of the two modes (normal or scan). Figure 5 shows the structure of the FFs when the circuit is operated in the normal mode. In the test or scan mode, all the FFs are disconnected and reconfigured as one or more shift registers called scan chains or scan registers. In the test mode all the state inputs (y_1, y_2,… y_k) become pseudo-primary inputs to the circuit. The state inputs to the combinational circuit are the present states of the FFs and the state outputs of the combinational circuit (Y_1, Y_2, …,Y_k) are the next states of the FFs. When developing tests for the FSM we assume we have only combinational circuit with the following inputs: x_1, x_2,…,x_n and y_1, y_2,… y_k; and outputs: z_1, z_2,…z_m and Y_1, Y_2, …,Y_k.

During test application, the FFs are initialised to put them in a known state. After initialisation the test patterns are applied to the primary inputs of the circuit, the results are latched at FFs and they are propagated to the output by placing the circuit in the test mode and clocking enough times to capture the results. This configuration makes the pseudo primary inputs as control inputs and the input (pseudo outputs) to a FF an observation point. To switch between normal operation and shift modes, each flip-flop needs additional circuitry to perform the switch

Boundary scan method was developed primarily for the testing of circuit boards and is defined by the core reference IEEE standard 1149.1-2001 "Test Access Port and Boundary-Scan Architecture". The idea to bring back the access to device pins by means of an internal serial shift register around the boundary of the device is accredited to European test engineers under the aegis JETAG (Joint European Test Action Group). When North American test engineers joined the group was named JTAG (Joint Test Action Group). It was this group that converted the ideas into an International standard, the IEEE 1149.1-1990 Standard first published in April 1990. The ICs that are compliant to this standard must incorporate extra hardware (Shift-Registers – Boundary scan registers) to facilitate communication between them and the board during testing. This idea is illustrated in figure 6.

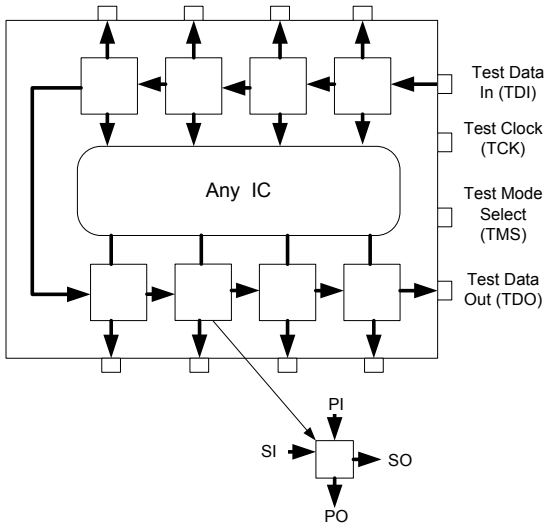

Fig. 6. Generic Boundary Scan Architecture

It is important to note at this point that the use of boundary scan has found their ways in internal testing and running of BIST. Apart from BISTs boundary scan is very useful in testing System on chips (SoC) in a new testing environment that enable systems with IP cores to be easily tested.

Up to this point we have considered techniques that require external generation and application of test patterns by an external device like automatic test equipment (ATE). BISTs are true DFT technique. It encompasses test generation, test application and response verification. It is very useful for current technology which requires testing at speed with due consideration to interconnect delays. Where SAF model fails, BIST succeeds. BISTs can detect faults that otherwise would not have been detected using SAF models – delay faults. In this methodology, test patterns are generated and test responses are analyzed on-chip.

The test pattern generator (TPG) in a BIST is implemented with linear feedback shift registers (LFSR) which is a finite state machine. It is a shift register with feedback from the last stage and other stages. The outputs of the flip-flops form the test pattern. It consists of FFs and XOR gates. The number of FFs and XOR gates depends on the characteristic polynomial of the LFSR. The generic BIST architecture is shown in figure 7. The responses of the circuit under test (CUT) could be large. Consequently the output responses are compacted by the response compactor (RC) to generate a signature at the end of the test application since we are interested on how the circuit responded to the various test patterns from the LFSR.

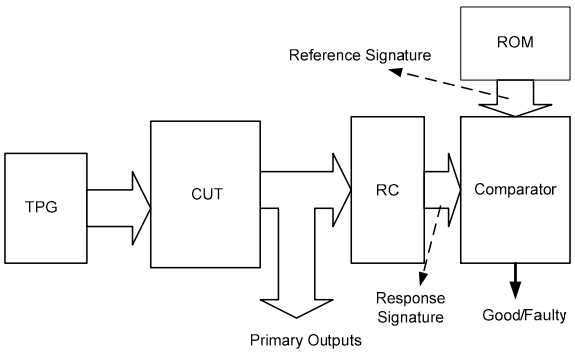

Fig. 7. General BIST Architecture

The generated signature is compared with the reference signature (signature of the fault-free circuit) to know whether the CUT is faulty or not. The detailed information on test generation and response compaction is beyond the scope of this paper. For more detailed information refer to [1], [8], [10] and [11].

VI. A Simple Example Of DFT Technique Using Scan Chain Methodology

As earlier mentioned DFT techniques help increase the testability of fabricated circuit by enhancing the controllability and observability of the various nets of the circuit. To show how DFT enhances the testability of a circuit, let us consider a simple counter circuit as shown in figure 8. The circuit is divided into two parts: combinational and sequential. The part containing the AND and XOR gates is the combinational circuit. The circuit has the following parts accessible to the outside world: outputs q0 to q2, Clock, Enable and Clear inputs. As it is now it will be difficult to properly test this circuit since we have no access to the internal nodes. If node n4 is stuck-at 1 or 0 there is no way we can know about this since we can neither control nor observe the node.

We are going to make this circuit testable by introducing some extra hardware and increasing the input and output ports. Firstly we replace the three flip-flops (FF) with a different type of FFs that has a multiplexer at the D input. By this action, additional three ports have been added namely: Scan-In, Scan-Out and Scan enable. The new sequential circuit is shown in figure 9.

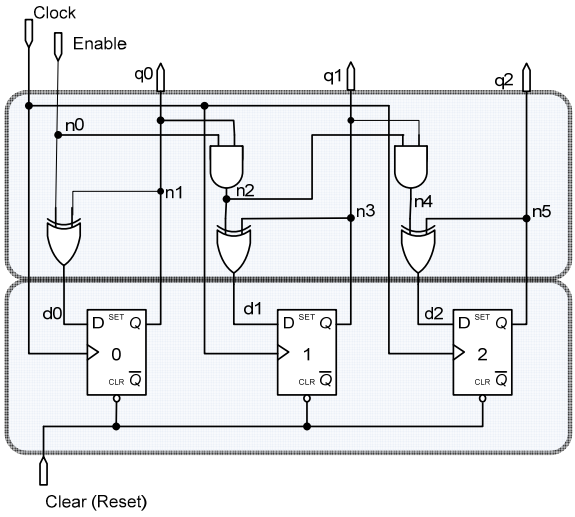

Fig. 8. A simple Counter Circuits

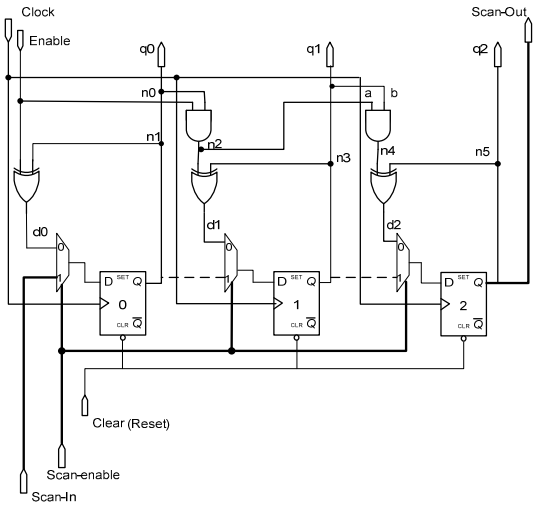

Fig. 9. A simple Counter circuits with DFT

With the new configuration the FFs form a shift register. The bit sequence can be shifted into the FFs through the scan-in input pin with the scan-enable signal set to high (logic 1) and the bits shifted out of the shift register can be observed at the scan-out output pin. Under normal operation of the sequential circuit the scan-enable signal is set to low (logic 0). The only change here is that our circuit can operate in two modes – normal and test modes. We can now develop and generate tests pattern for the combinational part to test the whole circuit the FFs inclusive. Let us assume that the node n4 is stuck-at-0. We can control input lines ‘a’ and ‘b’ to logic ‘1’ and set n5 to ‘0’ and observe the output at scan-out pin. The purpose of setting n5 to ‘0’ is to propagate the fault n4 stuck-at-0 to the output d2 of the XOR gate. Let us now look at how we can detect the fault stuck-at-0 at line n4.

Reset all FFs to 0

Set line ‘a’ =1 by setting enable input =1 and
n0=0 (FF0 was earlier reset to 0) d0=1,
Subsequently, FF0 output will be set to 1.

With enable=1 and FF0=1 => n2=1
Set line ‘b’ =1, by setting FF1 output to 1.
If n2=1, then d1=1 => FF1=1.
Set n5=0. Since n5 is the same as the FF2
output n5 is already 0.

With the above settings we are supposed to have logic 1 at the output. If however, the output is 0, then node n4 is stuck-at-0.

It is important to note that the functionality of the sequential circuit is not affected by the extra circuitry that implements the DFT technique. The major advantage of this modification is that testing of this circuit has become a combinational problem rather than a sequential one. The down side is that the circuit area has been increased, though not significantly.

VII. Conclusions

In this paper it has been shown that product quality depends to a greater extent on the thoroughness of verification and testing processes during its development. Testing of digital components/system is time consuming, expensive and can negatively affect time to market. The example given in this paper has clearly demonstrated that design for testability greatly eases the process of testing without a serious consequence on the area and delay issues of the would-be chip.

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Introduction to Adjustable Voltage-Range Current-Controlled Trapezoidal Waveform Generators

Mariusz Jankowski

Abstract — **The paper review series of circuits operating as trapezoidal waveform generators. All presented circuits share same rule of operation but offer different possibilities of their functionality enhancements. Enhanced versions provide ability to control voltage-range and differ slew-rates of rising and falling edges of output voltage waveform. Schematics, way of operation, and simulation results are presented.**

Index Terms — **Trapezoidal waveform generator, voltage-range limitation, slew-rate control.**

I. Introduction

Trapezoidal signal generation is a task useful in various analog [2] and some digital-related applications. There are numerous manners of generation of such signals. Some of them offer interesting features mainly due to untypical, namely current mode of processing leading to voltage-type output waveform. To change from current to voltage some kind of converter is required.

Usually what is recognized as a most obvious device of such type is simply a resistor. However, presented applications use a capacitor to integrate charge and produce proper voltage signal. Such approach is simple and enable various modifications, expanding original functionality over original operation principle.

II. Circuit Operation Overview

In practice this idea is known in various versions [1] and can be described as consecutive charging and discharging process of a load capacitor with two current mirrors consecutively sinking and sourcing current to and from this capacitor (Fig. 1).

Practically, current mirror output stages are use as current sources. Usage of constant value currents produces trapezoidal voltage patterns with constant slew-rate values. Voltage-range of generated voltage signal is limited by ground and supply voltage levels of feeding current mirrors.

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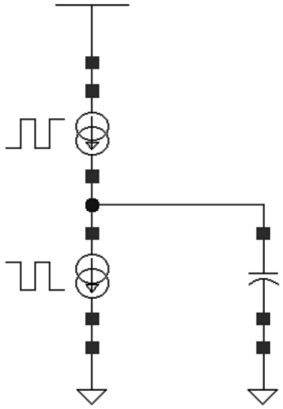

Fig. 1. Waveform generation idea

As shown earlier, trapezoidal waveform generator considered as a black box, on its output side should be seen as output sides of two switched current mirrors, both connected to a load capacitor or load capacitors. Such functionality may be obtained with wholly different internal structures. Differences between their internals are cause of various limitations of produces voltage patterns. Some structure can be simply reuses of subcircuits usually recognized as parts of quite different functional block.

III. OTA-based Generator

It can be argued that typical OTA amplifier (Fig. 2), due to current mode of inside signal transmission, can be used as a part of trapezoidal waveform generator [4].

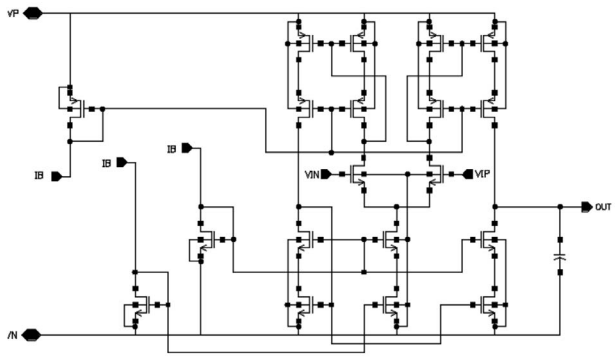

Fig. 2. OTA amplifier as a core of simple trapezoid generator

OTA is here used in open-loop configuration and its differential pair transistors are used as current switches. Such setup ensures that same current is consecutively sunk into and sourced from the output node. Capacitor presence at this node ensures proper operation of an OTA amplifier and produces trapezoidal waveform pattern on such capacitor.

Waveform produced by such structure is quite fixed in its shape (Fig. 3). Always one of the output current mirrors is on. Exception are conditions that working mirror is extinguished at its output side, or all the OTA is disabled. Also, both rising and falling signal edges slew-rate is same (Fig. 4). Any important changes in signal shape require hardware modifications inside or outside the OTA, like in [3], where additional external circuitry produces currents fed inside the OTA to produce modified output voltage signal.

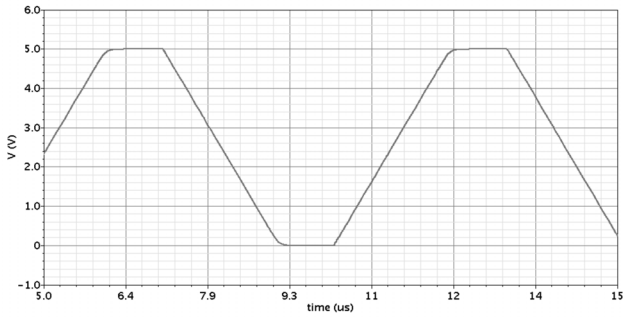

Fig. 3. Signal generated by simple current-controlled generator
Magnetization as a function of applied field

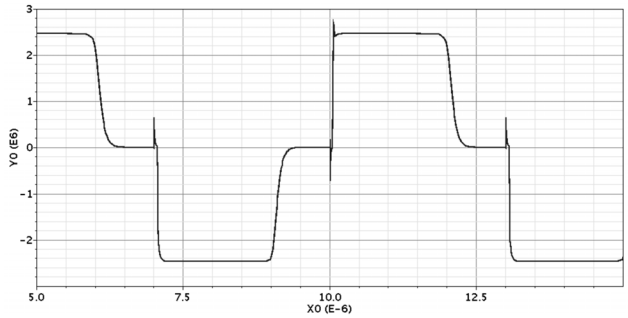

Fig. 4. Derivatives of signal presented in Fig. 3

As it is mentioned earlier, OTA is just one of possible solution of current feeding circuitry. As it is specialized for quite different applications, it is better to compose other circuitry providing both basic functionality and possibility of its expansion.

IV. Non-OTA Functional Equivalent

In general, current-controlled trapezoidal waveform generator may consist of only current mirrors and switches, formed into various structures. Exemplary structure [4] is presented in Figure 3.

This structure copies one input current to two complementary output mirrors. The current flow inside is driven with current switches. This structure is functionality similar to OTA with one noticeable exception. Inside the OTA a current flow never stop and always there is one conducting differential-pair transistor. Only during switching operation there can be short moment when none of differential-pair switches does not conduct current. This can be amended by means of shortly overlapping driving input signals.

In case of circuitry presented in Figure 5 switching process causes current mirrors preceding switches to go off completely, so when switch starts conducting again, the mirrors must regain proper operation mode. Apart from taking time it makes power consumption alter according to clock signal.

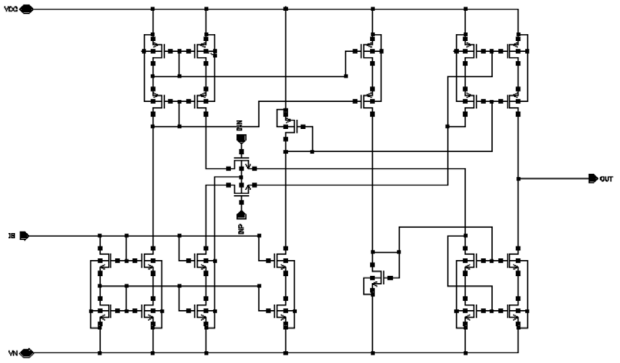

Fig. 5. Generator core with mirrors and current-blocking switches
Magnetization as a function of applied field

Exemplary improvement to this effect is shown in Figure 6. Here the currents inside the circuit are not extinguished but redirected. Power consumption stability is improved, though still there might happen moments when none of switches conducts. Overlapping driving signal can solve this problem as well as in case of OTA-based circuitry.

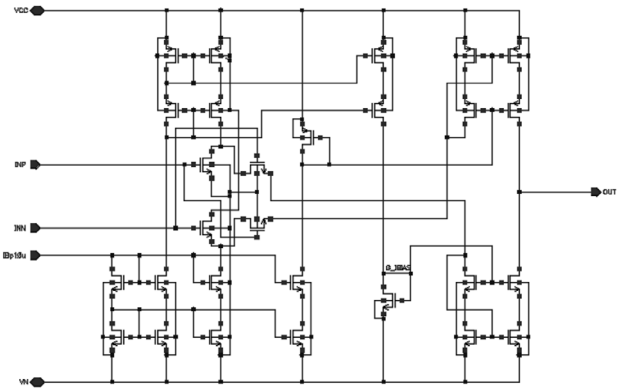

Fig. 6. Generator core with additional current-passing switches

V. Functionality Enhancements

Another approach to switching process is presented in Figure 7, here current flow is also controlled by switches, but here are no current-blocking switches. The switches works as current mirror input bypassing devices. When switch at the input of current mirror is off, current is copied to the output side of the mirror. Is switch is turned on, it

both bypass current mirror input, as a very low impedance circuitry and switches the mirror off due to shorting gate terminal of memory transistor to adjacent power net.

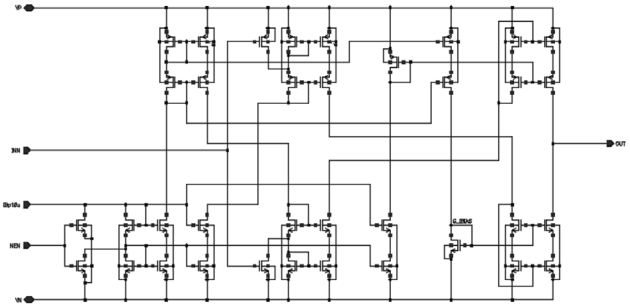

Fig. 7. Generator core with current-bypassing switches

Now, current flow inside the circuitry is uninterrupted, there are no time intervals during which there are no current receivers inside the circuit. There is always at least one way for current flow, at time there are two. Such mode of operation enable usage of only one driving signal.

All discussed, after some modifications, enable generation of waveform having different slew-rate values for rising and falling output signal edges. OTA-based circuits use one source of current, which is redirected according to switch operation.

In an OTA case, additional current adding circuitry should be added to achieve such functionality. In case of non OTA-based solutions, there is possibility of first producing or providing two current flows for distinct defining of slew-rate values and then proper directing of these DC currents to the output capacitor stage.

Also, placing the switching devices further away from the output stage enables utilization of another advantage related to current-mode signal transmission. Namely, the output current mirror stage can be supplied with different voltage levels. Thus, output signal voltage-range can be easily limited. Only piece of circuitry needed for this task is two simple voltage regulators. They can be based solely on OPAMPS, due to very limited power consumption of output stage power consumption of the waveform generator.

Fig. 8 circuitry is an enhancement of Fig. 7 waveform generator. It is equipped with two independent driving signals and two current inputs for output signal slew-rate definition, separately for rising and falling signal edge.

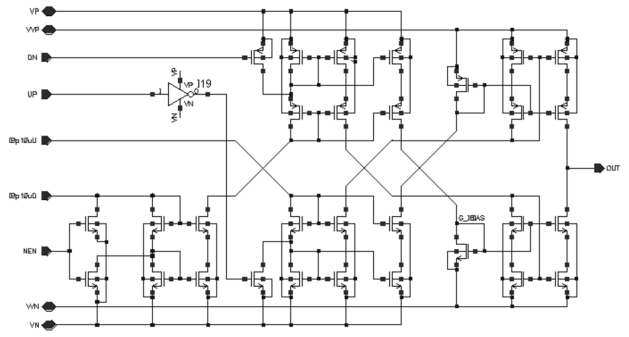

Fig. 8. Enhanced version of Fig. 7 circuit

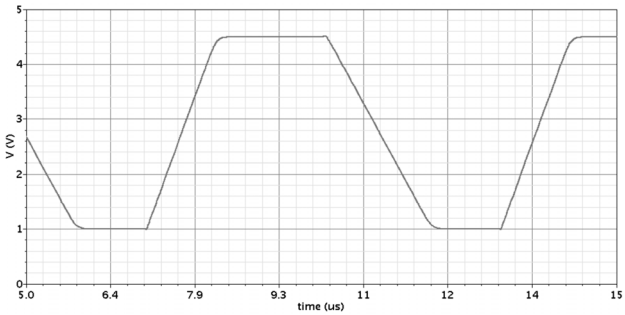

Fig. 9. Waveform produced with circuit from Fig. 8

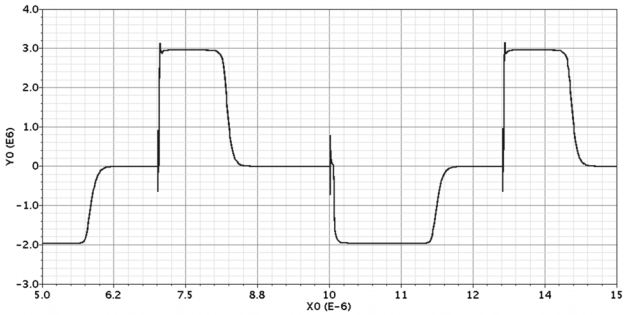

Fig. 10. Derivatives of waveform produced with circuit from Fig. 8 and presented in Fig. 9

Its output stage can be powered with different ground and supply voltage levels. All that is needed to enable this latest functionality is just to redraw the schematic in proper way and cut power nets at specific points.

This circuitry can be driven with two uncorrelated digital inputs and thus both output current mirror stages can be on same time. This feature can be very handy in some applications. For example there can be necessity of generation of signals having very low slew-rate during some time duration. This can be obtained by both enlarging the load capacitor and by minimizing current flow at the capacitor node. However, usually integrated capacitor value and shape is fixed and is not adjustable during circuitry operation. If it is, is poses other problems, big capacitance means big capacitor, which is not good situation in an integrated circuit. On the other hand circuit operation with very small current value makes current signal quality deteriorate during processing process. Noise, disturbance and current coping errors become relatively more pronounced as compared to the proper current signal.

The solution is both using high-quality current mirrors and providing two reasonable value currents to the very load capacitor. As one current is sunk in to capacitor and the other is sourced from there, we have simple current retraction operation, which can produce small current flow to and from the load capacitor. Fig. 9 shows exemplary signal produced by circuitry presented in Fig. 8. Two different slew-rates can be observed. Fig. 10 shows derivatives of the output signal.

What can be observed in generated waveforms presented so far, is rounded shape of the output voltage signal as it approaches its limit voltage. It is caused by fact, that

voltage-range limitation is obtained by means of extinguishing output stage current mirror, which happens gradually. Current mirror transistors leaves the saturation region, passes through linear region and then finally go off. The shorter transistor channel length the more abrupt current flow transition and less rounded output waveform signal. Unfortunately, shorter channel length means worse stability of current produced by the mirror against change of output waveform voltage level.

The situation can be bettered by using other means of voltage-limit functionality implementation. Such modification way is possible by means of output voltage control and comparison to required limit level. In case when limit voltage is reached, the capacitor loading current is switched-off, which is much faster operation then current-mirror self-extinguishing process. Simulation showing shape of output waveform produced this way is presented in Fig. 11.

Figure 12 presents derivative of Fig. 11. It can be seen that when generator output waveform reaches its lower voltage limit, its slew-rate (derivative) value changes to zero in much more rapid way than in situation observed when output waveform reaches its upper voltage limit. The first process is realized by voltage level control and loading current removal, the latter is performed by a process of current mirror self-extinguishing. Improvement in circuits performance can be easily noticed.

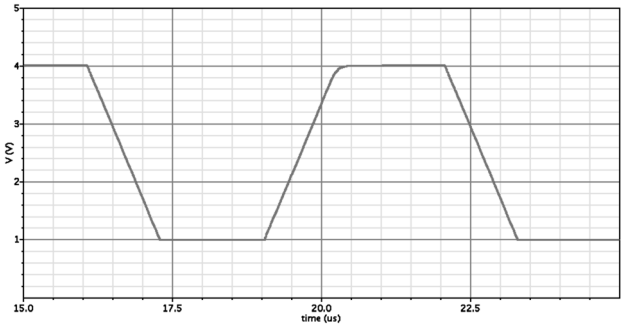

Fig. 11. Waveform created with modified way of voltage-control

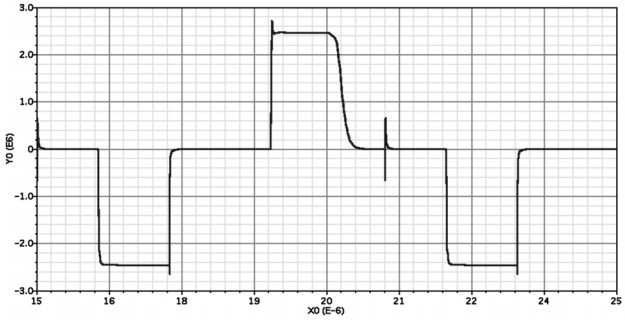

Fig. 12. Derivative of waveform presented in Fig. 11

VI. Conclusion

In the paper set of trapezoidal waveform circuits has been shown. All they operate using same simple principle. Proper choice of internal structure enables additional functionality enhancements being achieved without important drawbacks.

Number of possible enhancements in connection with still simple and consistent internal structure, widens field of application for such circuits.

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J2EE in Applications Supporting Business Management

Marcin Trojanowski, Wojciech Zabierowski, Andrzej Napieralski

***Abstract*—The article presents an example of application, which could be used to support the work of a company that must deal with improvement and evalution of knowledge of their workers. Application provide rich client graphical interface that facilitate navigation. The core of the system is based on Spring services, which support application in business logic. On the bottom of the application is middle tier Hibernate. Thanks to this design the system is very scalable and flexible**

***Index Terms* — JEE, Spring, Richfaces, Hibernate, Evaluation Manager**

I. Introduction

The scale of the flow of data in enterprises and institutions, with which we are now dealing with, strongly enforces the implementation and continuous modernization of the tools. Only in this way can avoid corrupting the information chaos. An efficient system allows you to control virtually every element of the company, especially helping the administration and management. Effective and well thought out tools facilitate the rapid development of the company, and used more elements so bravely. Artificial intelligence makes pre-engineered systems are becoming more flexible.

Information systems are a very wide area; an attempt to create a single coherent system that supports the entire process of the company is currently unrealistic. Today has not been created yet such a system, there are standards such as Product Lifecycle Management, which cover the entire production cycle; however, the implementation of a system does not exist.

At a time when companies need to quickly adapt to a changing environment should be ensured about the quality of the knowledge of their employees. Particularly important is the ability to quickly gather information in the computer industry. Excellent tool to achieve the trained staff can assist the process of testing the system. In this paper, an information system is limited to applications for conducting testing of employees in the company. The system is called Ewaluation Manager.

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II. Evaluation Manager Application

Imagine company that deals with IT technology that is very specific and it is not possible to acquire it on study or any commonly available market sources. This company employing new laborer will have to deal with teaching and evaluation of this unique technology. Evaluation Manager is the application that supports company with this process. Senior engineer can easily create evaluation test and assign it to appropriate employee. Then management can go through of done tests and result to choose best employee for given project.

III. Structure of the Application

Thanks to the construction of skeletons of the system is compatible with the MVC pattern. Each part of the application is strictly separated and forms a separate unit that can be replaced at any time without affecting other. A separation of the system architecture shows Fig.1.

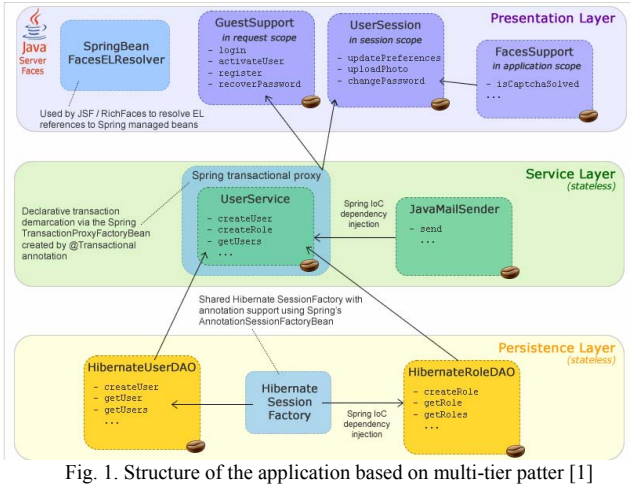

Fig. 1. Structure of the application based on multi-tier patter [1]

Application implements the three-tiered architecture, very characteristic to all JEE systems. The most top one is "Presentation Tier". The presentation tier displays information related to such services as i.e. browsing tests, creation tests, assigning test and pass tests. It communicates with other tiers by outputting results to the browser/client tier and all other tiers in the network.

In the common 3-tier architecture, the business logic in theory occupies the middle tier, the business-services tier or business layer. In practice, the business logic is often interwoven in the other two tiers (the user services tier and the database services tier), such as by encoding business logic in stored procedures and in decisions about input validation and display formatting. In Evaluation Manager Service layer is responsible for communication with Hibernate and making all calculation i.e. if employee pass or failed test.

The bottom layer is “Persistence Layer”. The persistence layer is an architectural layer whose job is to provide an abstract interface to information storage mechanism(s). An API to such an interface should be abstract, and independent of storage technologies and vendors. It would typically have features such as the following:

– Store / retrieve of whole object networks by key;

– Logical database cursor abstraction for accessing some / all instances of a given type;

– Transaction support – open, commit, abort Session management [2].

IV. Data Model

The data of the whole enterprise system is stored in a relational database on H2 database. H2 Database offers outside the SQL language, whose syntax and features are very similar to the database, Oracle, the ability to create stored procedures and triggers in Java. The asset base is built-in Web server that provides an administration console, which makes it easier to work with the database.

V. Service Tier

Creating complex programs is not easy now. The overwhelming presently prevailing triad faster, better, cheaper, much more complicated task. On the other hand, conventional systems will always be part of such an application, which is essential for the proper functioning of the application, but is not closely related to its business logic, in addition, it is repetitive and sometimes just boring to write. The skeleton of software development Spring is one of the main open source structures to improve and accelerate application development JEE. Spring was founded in 2003 on the basis of a license, "Apache 2.0 license." This template was created as an alternative to programming applications using EJB. Programming with Enterprise JavaBeans imposes many restrictions, while Spring provides the ability to create small and large applications with the proportionate amount of work. Cooperation with the Spring allows to focus around business application logic and not delving into the side steps. The modular architecture allows applying the framework in any configuration. An application can use not only the simplification of database transactions, but also support the creation of presentation.

Additional part of Service Tier used in Evaluation Manager is Spring Security. Spring Security is one of the Spring Modules project providing comprehensive security services for J2EE applications. Spring Security was created with an emphasis on projects built on the skeleton of Spring. There are two main application areas in which Spring Security is dominated by "authentication" and "authentication" (or "access control"). Authentication is a process in which users are defined that can perform actions on the application. Authorization is the process of determining whether a user can perform actions within the application. To get to the point where the authorization decision is needed, the identity of user has already been fixed in the authentication process. These concepts are characterized most web applications and are not unique to Spring Security.

The process of authentication for Spring Security is as follows:

1. The user visits a page and clicks on the link, whose entry requires authentication.
2. Request is sent to the server and the server determines that the user requests access to the source, which requires authentication.
3. In the event when the user is offline, the server sends a reply that the user must log on.
4. Depending on the implementation, the browser or redirect to a page with authentication, or authentication of such charge Cookie (web cookies.)
5. The browser sends a reply to a server in a HTTP POST containing the authentication data.
6. The server will decide whether the data are correct.
7. Request authentications will be invalidated and removed from memory.

In the Evaluation Manager Spring Security is mainly used to separate actions based on Roles. Role Admin has rights to create user with appropriate roles (role USER and SUPERVISOR. User of role SUPERVISOR has rights to create and assign tests. User of role USER supposed only to go through the assigned test.

VI. Client Tier

Evaluation Manager can be accessed only through web browser. This is most suitable and easy way. Currently market trends tend to avoid standalone clients. Evaluation Manger client tier is based on Richfaces framework. RichFaces is also open source project that adds functionality to existing Ajax applications using JSF without JavaScript leveraging the functionality of RichFaces JSF lifecycle management of objects, data validation and management of static and dynamic resource applications. Due to the fact that the components are integrated with the RichFaces Ajax is clear that the use of JSF acquires new dynamic properties (Fig. 2) [3].

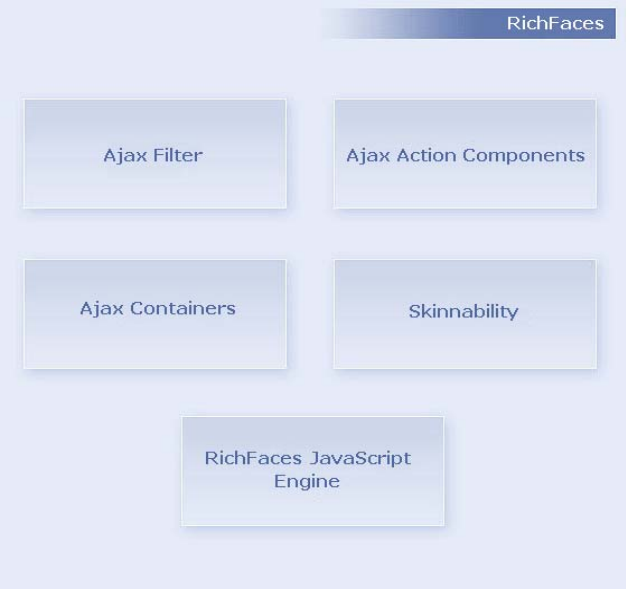

Fig. 2. Richfaces Architecture

Due to the fact that Evaluation Manager was implemented to satisfied to functional aspects Test Creation (Fig. 3, 4) and Passing Tests it is possible to divide Evaluation Manager into two functional modules. First one is responsible for creation of the test and assignment to particular user. Only user with role SUPERVISOR can create and assign test.

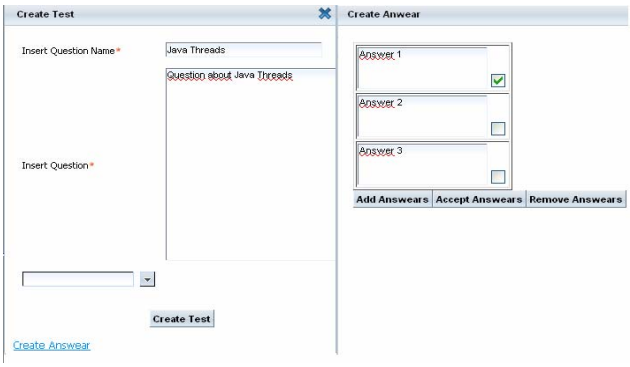

Fig. 3. Creation of the test

Fig. 4. Test assignment

The second module is responsible for passing through created test. Only user with Role USER can get assignments to pass (Fig. 5).

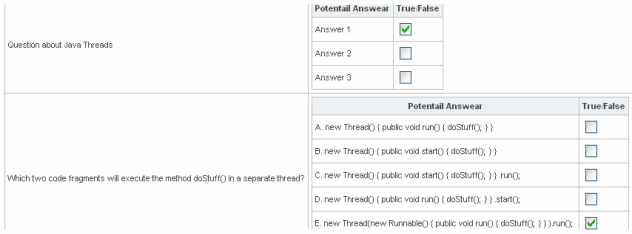

Fig. 5. Pass test

At the end SUPERVISOR can see what the status of all assignments is.

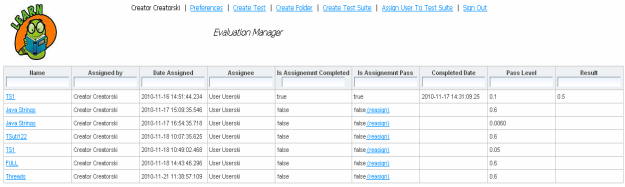

Fig. 6. Status of all assignments

VII. SUMMARY

The creation of this application has two goals. First is the fact that idea of Evaluation Manager can be used in real life company to support evaluation of new higher. The second goal was to present the abilities of current IT technologies which are non commercial but has enterprise abilities.

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System for Transmitting HDTV over IP Networks Using Open-Source Software

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Abstract – **The article presents results of work in the field of transmission of standard and non-standard high definition television signals over IP networks for application in medical environment. An example system for realtime signal acquisition, compression and broadcast is presented. It was built from off-the-shelf computer equipment, as a part of a video consulting system for medical (cardiological) purposes. To complete the task a DirectShow filter imitating a video capture device driver for Microsoft Windows operating system has been created.**

Index Terms — HDTV, DTV, digital video compression, IP, Internet

I. Introduction

UP until recent years the process of realtime compression of video materials in higher than standard definition was out of reach for PC users. The growth of computational power in general purpose microprocessors and the introduction of multi-core parallel processing made on-the-fly software compression and decompression possible [3]. In the year 2006 when the project started, it was already possible to perform the realtime compression, however there were just a few frame grabber devices available, that could perform full motion capture of HD video signals. Most of them were very expensive, and on the downside, the support for standard multimedia device access methods like DirectShow or Video4Linux under Windows and Linux operating systems was nonexistent. The software supplied with Matrox Solios XA frame grabber, which was available for tests and development, allowed capturing still images and video sequences to file, but no further live video processing was available, including forwarding the stream to other applications.

II. Technical Requirements

- On the transmitter side, the system has to work under Windows XP.
- Must ensure stable and uninterrupted transmission for minimum 12 hours.
- Input interfaces must include Matrox Solios XA and internal sound card of the transmitter PC.
- Standard XGA signal coming from Kramer VP-725DS scaler will be processed.
- A video codec, which will ensure smooth 1024x768 stream at 60 fps has to be used.
- Artifacts introduced by the video codec should be imperceptible to the user.
- Both parties of the video link have to see and hear each other. The system should allow uninterrupted conversations between them.
- Full bandwidth must not exceed 30 Mbit/s.

III. Research

The lack of DS and V4L support prevented frame grabber devices from being used together with publicly available video encoding software such as open-source FFMPEG, MPEG4IP, VideoLAN, MEncoder and proprietary Windows Media Encoder or Flash Media Encoder as a mean of HDTV signal webcasting.

From two possible approaches – writing an encoding application from scratch or creating a universal interface for use with any standard multimedia application, the latter was selected. The frame grabber was acquired with a software development kit for Microsoft Windows only. A fast research showed, that the fastest way to implement the interface between the device and software would be to create a userspace DirectShow filter. This would allow the use of VideoLAN Client application as the transmitter and receiver of the audio-video stream.

Such DirectShow filter [2] (so called "source filter") has been created in course of the project, using MIL-Lite programming libraries for the Matrox frame grabber, and Microsoft Windows SDK, which include a sample video stream generating filters ("PushSource" and "Ball"), which can give a good idea on how to write your own source filter. The missing information about registering the filter in the system registry, so that it is seen by the system as a video capture device was obtained from microsoft.public.win32.programmer.directx.video newsgroup.

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IV. The System

Two independent communication channels were established: the main HD stream from the operating room, and a lower quality and low bitrate return channel carrying video, sound from the conference venue. The technical crew was provided with text messaging using the same channel (Fig. 1).

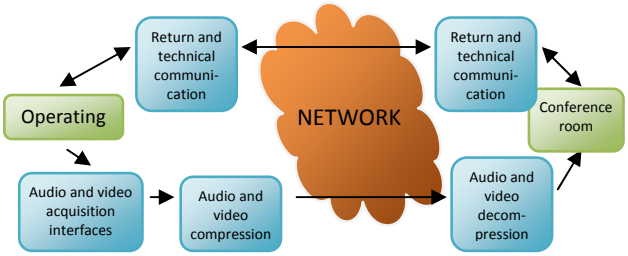

Fig. 1. Complete video consulting system schema

There were three video sources on site at the operating room: HDTV camera, digital angiography device, and electrocardiography recorder, each with different resolution and refresh rate. All input signals in the operating room were scaled down to 1024x768 resolution and 60 Hz refresh rate using Kramer VP-725DS scaler/switcher (Fig. 2). This exact resolution was chosen because multimedia projectors available on the remote location had XGA native resolution. Unification of resolutions also had to be done because there is no way of determining the parameters of the signal coming into the exact frame grabber card used in the project, basing on the data provided by the frame grabber itself. The user has to know the parameters to perform a successful capture in the first place.

Audio and video digitization was done on a dual processor Intel Xeon based PC equipped with Matrox Solios XA frame grabber and an AC'97 compatible motherboard integrated soundcard.

The frame grabber is a 64-bit PCI-X card based on Altera Stratix FPGA chipset. It has 4 independent 10-bit input A/D converters. They can be linked to form two dual signal input (S-video) or a single three signal YUV/RGB component video input. The maximum capture resolution is 1024x1024 pixels, and pixel clock rate of 65 MHz [5], provided the pixel clock signal is fed directly to the card. In case of a computer video signal with standard VESA timings and VGA signaling, the maximum resolution is 1024x768 at 60 Hz refresh rate (pixel clock rate of this signal is exactly 65 MHz) [4].

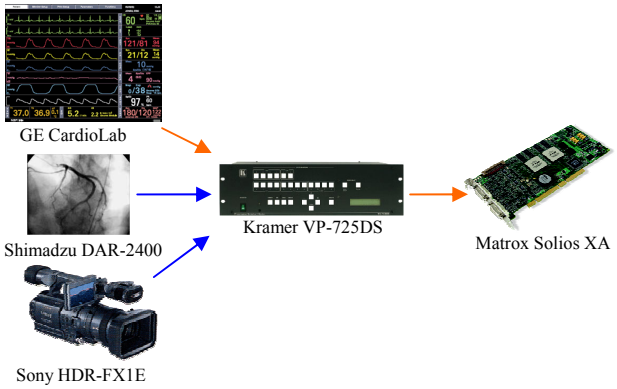

Fig. 2. Video signal paths and interfaces. Blue – component video, orange – RGB

VideoLAN Client (version 0.8.6) was used for encoding the video and audio signals, because of its flexibility. To minimize IP overhead and benefit from near-lossless network, UDP protocol was used. After numerous tests with different codecs, multiplexers and bitrate, a decision was made to set the bitrate level at 8 Mbit/s, and use MPEG-4 Simple Profile codec for video and MPEG-1 Layer 1, 192 Kbit/s for audio with MPEG Transport Stream multiplexing. An example stream made using these parameters was shown to the medical staff, and their decision was that the picture doesn't loose any important details and can be used for medical diagnosis.

Fig. 3. Cardiac surgery seen from the conference venue. HD feed on the left, and the return channel on the right

Because only one frame grabber card was available, for the return channel a software videoconferencing solution was considered. Tests with various open-source H.323 and SIP clients were unsuccessful because of their low stability and the choice fell on free Skype software. Should the high definition channel fail, a possibility to continue the webcast with the emergency usage of Skype's video call function was available.

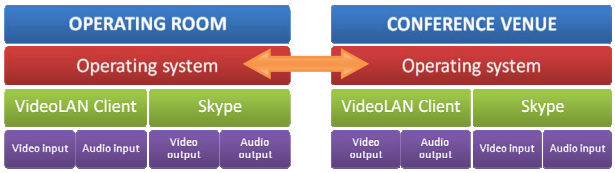

Fig. 4. Final system's architecture

The delay measured was approximately 2 seconds on the HD channel, and under 100 ms for the return channel. Various literature including [1] mentions a tolerable latency value of 200-300 ms over which the communication between two people is starting to be perceived by them as "uncomfortable".

V. Conclusion

It has been shown, that currently available PC computers are able to perform realtime compression of HDTV signals using open-source software solution. Currently there are devices on the market that allow VGA capture using DirectShow compatible drivers, meaning that most effort described in the article could be spared. It was observed, that the MPEG-4 encoder implementation in VideoLAN Client doesn't fill the defined bandwidth. Current choice of codecs could also be revised. As H.264 provide lower bitrate while maintaining the same overall picture quality it would be advisable to switch to the new codec. What is more, the open-source implementation of this codec, x264 since march 2010 is optimized for low latency encoding. Latency is a crucial factor for video conferencing and video consulting applications. Currently obtained latency makes interaction between two locations a quite challenging task, and without some amount of training it's not possible to have a fluent conversation. The VideoLAN Client wasn't designed for low latency processing, so further improvements would include replacing it with another application, possibly FFMPEG.

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Method of Binary Structures Compression on Basis of Cascade Encoding in Telecommunication Systems

Barannik V.V., Hahanova A.V.

Annotation – **Grounded, that due to presentation of binary array as integral structure as a cascade structural number, additional reduction of structural surplus is provided. A cascade structural number is the number which satisfies limits on the number of units carouses and on the dynamic range of one-dimensional floating structural numbers (OSN) codes. The theorem is proved about forming of cod-number for a cascade structural number. It is shown, that amount of digits on presentation of binary column, which is examined as an element of cascade structural number less than, amount of digits on presentation of that column, but examined as a one-dimensional floating structural number.**

I. State of Problem and Analysis of Literature

The features of information treatment in the telecommunication systems consist of treatment uneven binary sequences are given. Sequences have an arbitrary structure and different statistical descriptions. For the telecommunication systems different intensity of traffic, origin of turns and duplication packages, are characteristic. It results in the additional increase of information volumes, processed and transferable in the telecommunication systems (TCS) [1]. Such circumstances are reason of leading time increase to information. From here is the scientifically-applied task which consists in diminishing of binary information volumes in TCS.

Direction of task decision consists in organization of binary information compact presentation [2 - 5]. One from the effective methods of compression is based on the one-dimensional structural encoding [6]. However for such encoding there is failing. Failing consists of amount M digits on a code view C_ν determined, as $M = [\ell og_2 V_{\nu,\eta}] + 1$ beaten. From other side for the value of code inequality can be executed

$$C_\nu <<< V_{\nu,\eta}. \quad (1)$$

Then for the real length $\ell og_2 C_\nu$ codegrams a condition is executed

$$\ell og_2 C_\nu <<< [\ell og_2 V_{\nu,\eta}] + 1. \quad (2)$$

Plenty of no significant digits, equal, appear in this case $[\ell og_2 V_{\nu,\eta}] + 1 - \ell og_2 C_\nu$ to the bats. Such amounts of digits are surplus and results in the decline of binary matrices ratio aspect.

It means that it is needed to provide the additional increase of compression information degree in the conditions of arbitrary binary structure. Therefore the purpose of researches consists of method compression development without loss of information on the basis of account two cascade structures of binary arrays.

II. Basic material

We will consider the removal of failing, which was related to the choice of large length codegram on presentation of one-dimensional structural number cod-number. It is suggested to examine the aggregate of separate binary columns (OSN of numbers) taking into account additional limits on their dynamic ranges

$$C_\nu <<< \lambda_\nu. \quad (3)$$

In this case binary arrays are examined as integral structural objects.

Determination 1. By the cascade structural number $G^{(2)}$ binary arrays are named (sequence of columns, made from binary elements $g_{k\ell} \in [0;1]$), the columns of which are one-dimensional floating structural numbers which the number of units carouses is certain for

$$G^{(\ell)} = \{g_{k\ell}\}_{k=\overline{1,n}} \to \eta_\ell, \quad (4)$$

and values of codes-numbers C_ℓ limited from above by sizes $F(\eta,\lambda)_\ell$:

$$C_\ell < F(\eta,\lambda)_\ell = \min(V_{\ell,\nu,\eta}; \lambda_\ell), \ \ell=\overline{1,n}. \quad (5)$$

Determination 2. By the great number $\Omega^{(2)}_{n,\eta,\lambda}$ possible cascade structural numbers (CSN) a great number, which consists of two regularities binary arrays which terms are executed for, is named:

1) number of units carouses for ℓ column of array equal η_ℓ, $\ell=\overline{1,n}$;

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2) size of code C_ℓ, formed for ℓ OSN, limited from above by a size $\min(V_{\ell,\nu,\eta};\lambda_\ell)$, $\ell=\overline{1,n}$.

For determination of great number volume $\Omega^{(2)}_{n,\eta,\lambda}$ we will formulate and will prove a next theorem.

The theorem about the great number volume cascade structural numbers. Amount $V^{(2)}_{n,\eta,\lambda}$ cascade structural numbers which satisfy limitations (4) and (5), equal

$$V^{(2)}_{n,\eta,\lambda}=\prod_{\ell=1}^{n}F(\eta,\lambda)_\ell, \qquad (6)$$

$$F(\eta,\lambda)_\ell=\min(V_{\ell,\nu,\eta};\lambda_\ell),\ \ell=\overline{1,n} \qquad (7)$$

$$V_{\ell,\nu,\eta}=(\nu+1)!/(2\eta_\ell)!\ (\nu+1-2\eta_\ell)!, \qquad (8)$$

where η_ℓ – value of units carouses number for ℓ OSN of binary array; ν – length of OPSCH, in special case equal $\nu=n$.

Proof. As on the first cascade columns of CSN are OSN of number, that value of their code is even C_ℓ.

From other side of size C_ℓ are array cells C.

Then there are variants, when one of inequalities are executed

$$\max_{1\le\psi\le\Psi}\{C_{\ell\psi}\}+1<V_{\ell,\nu,\eta}$$

or

$$\max_{1\le\psi\le\Psi}\{C_{\ell\psi}\}+1\ge V_{\ell,\nu,\eta}.$$

Therefore size C_ℓ will limit by $F(\eta,\lambda)_\ell$:

$$C_\ell<F(\eta,\lambda)_\ell=\begin{cases}\lambda_\ell, & \to\lambda_\ell<V_{\ell,\nu,\eta};\\ V_{\ell,\nu,\eta}, & \to\lambda_\ell\ge V_{\ell,\nu,\eta}.\end{cases}$$

The amount of sequences, on the value of elements which limitations (4) is imposed and (5), is equal to the amount of transpositions with reiterations with limits on the dynamic range elements. The theorem is well-proven.

From the well-proven theorem about a volume $V^{(2)}_{n,\eta,\lambda}$ great numbers $\Omega^{(2)}_{n,\eta,\lambda}$ cascade structural numbers investigation flow out.

Investigation 1. For any known sizes η_ℓ, $\ell=\overline{1,n}$ has gotten for the sequence of one-dimensional floating structural numbers inequality, is executed between sizes $\sum_{\ell=1}^{n}\ell og_2V_{\nu,\eta_\ell}$ and $\ell og_2V^{(2)}_{n,\eta,\lambda}$:

$$\ell og_2V^{(2)}_{n,\eta,\lambda}\le\sum_{\ell=1}^{n}\ell og_2V_{\nu,\eta_\ell}. \qquad (9)$$

where $\sum_{\ell=1}^{n}\ell og_2V_{\nu,\eta_\ell}$ – maximal total amount of digits on presentation sequences of OSN, which are examined as separate numbers;

$\ell og_2V^{(2)}_{n,\eta,\lambda}$ – maximal amount of digits on presentation of OSN sequence, is examined as a cascade structural number.

It means that as a result of cascade number forming on the basis of separate OSN reduction of digits amount is provided on their presentation in relation to an initial variant. This condition is executed taking into account situations, when $C_\nu<<<V_{\nu,\eta}$.

For forming of code a cascade structural number must develop the proper process of possible binary combinations numeration which belong to the great number $\Omega^{(2)}_{n,\eta,\lambda}$.

For this purpose we will formulate determination.

Determination 3. Cascade structural numeration of information is named the process of sequence number calculation, which occupies a cascade structural number in a possible great number $\Omega^{(2)}_{n,\eta,\lambda}$.

For the binary array $G=\{g_{k\ell}\}$, $k=\overline{1,n}$, $\ell=\overline{1,n}$, $g_{k\ell}\in\{0;1\}$, examined as CSN could be formed code $C^{(2)}$, which is calculated on the basis of expressions:

$$C^{(2)}=\sum_{\ell=1}^{n}(\sum_{k=1}^{n}g_{k\ell}\,p_{k\ell})\prod_{\phi=\ell+1}^{n}F(\eta,\lambda)_\ell; \qquad (10)$$

$$g_{0\ell}=0,\ \beta_{0\ell}=2\eta_\ell,\ \beta_{k\ell}=\beta_{k-1,\ell}-\left|g_{k-1,\ell}-g_{k\ell}\right|, \qquad (11)$$

where $p_{k\ell}$ – value of gravimetric coefficient of element $g_{k\ell}$ one-dimensional floating structural number; n – an amount of binary elements is in OPSCH; $\beta_{k\ell}$ – recurrent parameter, equal to the amount of binary overfills (transitions between «0» and «1») for a sequence which consists of $(n-k+1)$ untilled elements.

For the construction of cascade code constructions $C^{(2)}_\psi$ required:

– to build arrays C, which consist of codes C_ν separate OSN values;

– to conduct the selection of dynamic ranges on the lines of array C.

The construction of the second cascade of code constructions is carried out in other words.

Determination 4. The cascade code constructions of OSN are named code constructions which are formed as a result of codes construction for an aggregate one the regularity of floating structural numbers.

Array C has the following kind:

$$C=\begin{vmatrix}C_{11}\ \dots\ C_{1\psi}\ \dots\ C_{1\Psi}\\ C_{\ell1}\ \dots\ C_{\ell\psi}\ \dots\ C_{\ell\Psi}\\ C_{n1}\ \dots\ C_{n\psi}\ \dots\ C_{n\Psi}\end{vmatrix},$$

where $C_{\ell\psi}$ – code of one-dimensional floating structural number, formed on a base ℓ column ψ binary array; Ψ – amount of binary arrays for which cascade code

constructions are formed.

The process of the cascade structural encoding includes the followings stages:

1. One-dimensional structural floating numbers are built by taking into account implementation of terms:

$$\sum_{\ell=1}^{2}([\ell\log_2(V(\nu_\ell,\eta_\ell^{(\theta)}))]+1) \ \geq\ [\ell\log_2 V_{\nu,\eta}]+1;$$

$$[\ell\log_2\eta_{\max}+1]+1 \ \leq\ \sum_{\ell=1}^{2}([\ell\log_2\eta_{\ell,\max}+1]+1),$$

where $\eta_{\max}$, $\eta_{\ell,\max}$ – maximal values of carouses number of units for OPSCH, which have length accordingly equal ν and ν_ℓ.

In this case $\nu=n$. It is suggested for utilized $n=8$.

2. The redistribution of official information is conducted depending on values $V_{\nu,\eta}$ volumes of possible great number of OPS numbers. Correlations are utilized for this purpose:

1) for ν even and $\eta_{\max}$ even:

$$\eta_{cp}=0;\ \text{if}\ \eta>\eta_{cp},\ \eta=2(\eta-\eta_{cp})-1;$$
$$\text{if}\ \eta<\eta_{cp},\ \eta=2(\eta_{cp}-\eta);$$

2) for ν even and $\eta_{\max}$ odd:

$$\eta=\lceil(\nu+1)/4\rceil=0;\ \text{if}\ \eta>\lceil(\nu+1)/4\rceil,$$
$$\eta=2(\eta-\lceil(\nu+1)/4\rceil);$$
$$\text{if}\ \eta<\lceil(\nu+1)/4\rceil,\ \eta=2(\lceil(\nu+1)/4\rceil-\eta)-1$$

3) for ν odd and $\eta_{\max}$ even:

$$\eta_{cp}=0;\ \text{if}\ \eta>\eta_{cp},$$
$$\eta=2(\eta-\eta_{cp})-1;$$
$$\text{if}\ \eta<\eta_{cp},\ \eta=2(\eta_{cp}-\eta);$$

4) for ν odd and $\eta_{\max}$ odd:

$$\eta=\lceil(\nu+1)/4\rceil=0;\ \text{if}\ \eta>\lceil(\nu+1)/4\rceil,$$
$$\eta=2(\eta-\lceil(\nu+1)/4\rceil);$$
$$\text{if}\ \eta<\lceil(\nu+1)/4\rceil,\ \eta=2(\lceil(\nu+1)/4\rceil-\eta)-1;$$

3. For arrays the exposure of limits is carried out on dynamic ranges λ_ℓ, which are utilized for the calculation of gravimetric coefficients $F(\eta,\lambda)_\ell$:

$$\lambda_\ell=\max_{1\leq\psi\leq\Psi}\{C_{\ell\psi}\}+1, \qquad (12)$$

where λ_ℓ – limit on the range of sizes $C_{\ell\psi}$ in ℓ to the line.

4. Forming of codes is conducted $C_\psi^{(2)}$ second cascade level, formed for ψ column of array C on the basis of parameters $\psi=\overline{1,\Psi}$:

$$C_\psi^{(2)}=\sum_{\ell=1}^{n}(\sum_{k=1}^{n}g_{k\ell}^{(\psi)}p_{k\ell}^{(\psi)})\prod_{\phi=\ell+1}^{n}F(\eta,\lambda)_\phi; \qquad (13)$$

$$g_{0\ell}=0,\ \beta_{0\ell}=2\eta_\ell,\ \beta_{k\ell}=\beta_{k-1,\ell}-\left|g_{k-1,\ell}-g_{k\ell}\right|, \qquad (14)$$

where $g_{k\ell}^{(\psi)}$ – $(k;\ell)$ element ψ cascade structural number; $p_{k\ell}^{(\psi)}$ – gravimetric coefficient of element $g_{k\ell}^{(\psi)}$.

Next investigation follows from the features of cascade code structures forming.

Investigation 2. Value of code $C_\psi^{(2)}$ cascade structural number, where there will be a less size $V_{n,\eta,\lambda}^{(2)}$, which is equal to the total amount of CSN:

$$C_\psi^{(2)}<V_{n,\eta,\lambda}^{(2)}=\prod_{\ell=1}^{n}F(\eta,\lambda)_\ell. \qquad (15)$$

On the basis of the well-proven investigation 2 flows out, that for preset the parameters n, λ_ℓ and $\{\eta_1,...,\eta_\ell,...,\eta_n\}$ by the high bound of digits amount, which are taken on a code view $C_\psi^{(2)}$ cascade structural number, there is a size $(\ell\log_2 V_{n,\eta,\lambda}^{(2)}+1)$:

$$\ell\log_2 C_\psi^{(2)}<1+\ell\log_2 V_{n,\eta,\lambda}^{(2)}. \qquad (16)$$

Investigation 3. For the set values of sizes: lengths of OSN n, vector of limitations $F=\{F(\eta,\lambda)_\ell\}_{\ell=\overline{1,n}}$ and vector $\{\eta_1,...,\eta_\ell,...,\eta_n\}$ limits on the number of units carouses in the binary columns of cascade structural number, inequality is executed

$$\ell\log_2\overline{C}_\psi^{(2)}\ \leq\ \sum_{\ell=1}^{n}\ell\log_2 C_{\ell\psi}/n, \qquad (17)$$

where $\ell\log_2\overline{C}_\psi^{(2)}$ – middle on an amount n binary columns value of digits amount, which is expended on presentation of size $C_\psi^{(2)}$:

$$\ell\log_2\overline{C}_\psi^{(2)}=\ell\log_2 C_\psi^{(2)}/n; \qquad (18)$$

$\sum_{\ell=1}^{n}\ell\log_2 C_{\ell\psi}/n$ – middle amount of digits, which is expended on presentation of one column, examined as a separate one-dimensional floating structural number.

Thus:

1. It has grounded that due to presentation of binary array as integral structure as a cascade structural number additional reduction of structural surplus is provided. The cascade structural number satisfies limitations on:

– number of units carouses;

– dynamic range of OPSCH codes.

2. The theorem is well - proved about forming code for a cascade structural number. On the basis of the well - proved theorem the high bound is determined for the amount of digits, code of CSN taken on presentation.

3. It is well-proven that amount of digits on binary column presentation, examined as an element of cascade structural number less, than amount of digits on presentation of that column, but examined as the one-dimensional floating structural number.

III. Conclusion

1. The methodological bases of the binary cascade structural encoding are created. A cascade structural number is a two dimension array for which:

- at the level of binary columns consideration is conducted as structural floating numbers;
- at the level of codes-numbers of separate columns additional limits come to light on a dynamic range.

In this case binary arrays are examined as integral structural objects.

2. Numeration of cascade structural numbers, which allows forming a codegram for an arbitrary binary array, is developed, taking into account structural limitations on two cascade levels. It is grounded on the basis of the built numeration, that:

- due to presentation of binary array as integral structure as a cascade structural number, satisfying limits on the number of units carouses and on the dynamic range of OSN codes, additional reduction of structural surplus is provided;
- there is a high bound for the amount of digits, code of CSN, which is taken on his presentation;
- amount of digits on presentation of binary column, examined as an element of cascade structural number less, than amount of that column digits on presentation, but which is examined as an one-dimensional floating structural number.

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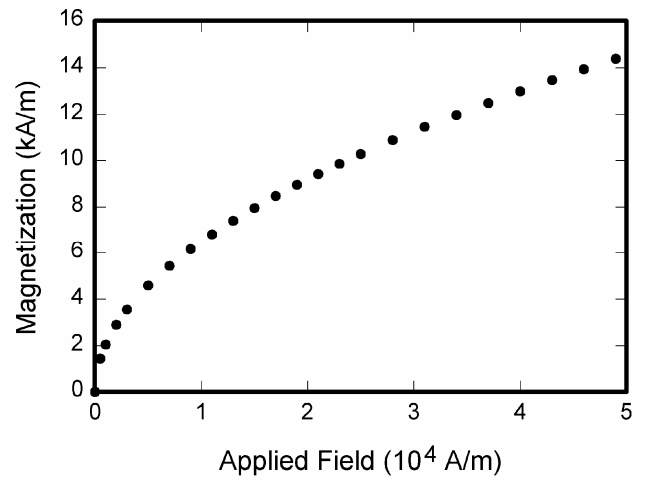

Fig. 1. Magnetization as a function of applied field. Note that "Fig." is abbreviated. There is a period after the figure number, followed by two spaces. It is good practice to explain the significance of the figure in the caption.

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TABLE I
UNITS FOR MAGNETIC PROPERTIES

Symbol	Quantity	Conversion from Gaussian and CGS EMU to SI [a]
Φ	magnetic flux	1 Mx $\rightarrow 10^{-8}$ Wb = 10^{-8} V·s
B	magnetic flux density, magnetic induction	1 G $\rightarrow 10^{-4}$ T = 10^{-4} Wb/m^2
H	magnetic field strength	1 Oe $\rightarrow 10^3/(4\pi)$ A/m
m	magnetic moment	1 erg/G = 1 emu $\rightarrow 10^{-3}$ A·m^2 = 10^{-3} J/T
M	magnetization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 10^3$ A/m
$4\pi M$	magnetization	1 G $\rightarrow 10^3/(4\pi)$ A/m
σ	specific magnetization	1 erg/(G·g) = 1 emu/g $\rightarrow$ 1 A·m^2/kg
j	magnetic dipole moment	1 erg/G = 1 emu $\rightarrow 4\pi \times 10^{-10}$ Wb·m
J	magnetic polarization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 4\pi \times 10^{-4}$ T
χ, κ	susceptibility	1 $\rightarrow 4\pi$
χ_ρ	mass susceptibility	1 cm^3/g $\rightarrow 4\pi \times 10^{-3}$ m^3/kg
μ	permeability	1 $\rightarrow 4\pi \times 10^{-7}$ H/m = $4\pi \times 10^{-7}$ Wb/(A·m)
μ_r	relative permeability	$\mu \rightarrow \mu_r$
w, W	energy density	1 erg/cm^3 $\rightarrow 10^{-1}$ J/m^3
N, D	demagnetizing factor	1 $\rightarrow 1/(4\pi)$

Vertical lines are optional in tables. Statements that serve as captions for the entire table do not need footnote letters.

[a]Gaussian units are the same as cgs emu for magnetostatics; Mx = maxwell, G = gauss, Oe = oersted; Wb = weber, V = volt, s = second, T = tesla, m = meter, A = ampere, J = joule, kg = kilogram, H = henry.

III. MATH

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IV. UNITS

Use either SI (MKS) or CGS as primary units. (SI units are strongly encouraged.) English units may be used as secondary units (in parentheses). **This applies to papers in data storage.** For example, write "15 Gb/cm^2 (100 Gb/in^2)." An exception is when English units are used as identifiers in trade, such as "3½-in disk drive." Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersteds. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity in an equation.

The SI unit for magnetic field strength H is A/m. However, if you wish to use units of T, either refer to magnetic flux density B or magnetic field strength symbolized as $\mu_0 H$. Use the center dot to separate compound units, e.g., "A·m^2."

V. Helpful Hints

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Figure axis labels are often a source of confusion. Use words rather than symbols. As an example, write the quantity "Magnetization," or "Magnetization *M*," not just "*M*." Put units in parentheses. Do not label axes only with units. As in Fig. 1, for example, write "Magnetization (A/m)" or "Magnetization ($\mathrm{A \cdot m^{-1}}$)," not just "A/m." Do not label axes with a ratio of quantities and units. For example, write "Temperature (K)," not "Temperature/K."

Multipliers can be especially confusing. Write "Magnetization (kA/m)" or "Magnetization (10^3 A/m)." Do not write "Magnetization (A/m) × 1000" because the reader would not know whether the top axis label in Fig. 1 meant 16000 A/m or 0.016 A/m. Figure labels should be legible, approximately 8 to 12 point type.

B. References

Number citations consecutively in square brackets [1]. The sentence punctuation follows the brackets [2]. Multiple references [2], [3] are each numbered with separate brackets [1]–[3]. When citing a section in a book, please give the relevant page numbers [2]. In sentences, refer simply to the reference number, as in [3]. Do not use "Ref. [3]" or "reference [3]" except at the beginning of a sentence: "Reference [3] shows ... ." Please do not use automatic endnotes in *Word*, rather, type the reference list at the end of the paper using the "References" style.

Number footnotes separately in superscripts (Insert | Footnote).[1] Place the actual footnote at the bottom of the column in which it is cited; do not put footnotes in the reference list (endnotes). Use letters for table footnotes (see Table I).

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Define abbreviations and acronyms the first time they are used in the text, even after they have already been defined in the abstract. Abbreviations such as IEEE, SI, ac, and dc do not have to be defined. Abbreviations that incorporate periods should not have spaces: write "C.N.R.S.," not "C. N. R. S." Do not use abbreviations in the title unless they are unavoidable (for example, "IEEE" in the title of this article).

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Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). First use the equation editor to create the equation. Then select the "Equation" markup style. Press the tab key and write the equation number in parentheses. To make your equations more compact, you may use the solidus (/), the exp function, or appropriate exponents. Use parentheses to avoid ambiguities in denominators. Punctuate equations when they are part of a sentence, as in

$$\int_0^{r_2} F(r,\varphi)\, dr\, d\varphi = [\sigma r_2 / (2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\, |z_j - z_i|)\, \lambda^{-1} J_1(\lambda r_2)\, J_0(\lambda r_i)\, d\lambda . \quad (1)$$

Be sure that the symbols in your equation have been defined before the equation appears or immediately following. Italicize symbols (*T* might refer to temperature,

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but T is the unit tesla). Refer to "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ... ."

E. Other Recommendations

Use one space after periods and colons. Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." [It is not clear who or what used (1).] Write instead, "The potential was calculated by using (1)," or "Using (1), we calculated the potential."

Use a zero before decimal points: "0.25," not ".25." Use "cm^3," not "cc." Indicate sample dimensions as "0.1 cm × 0.2 cm," not "0.1 × 0.2 cm^2." The abbreviation for "seconds" is "s," not "sec." Do not mix complete spellings and abbreviations of units: use "Wb/m^2" or "webers per square meter," not "webers/m^2." When expressing a range of values, write "7 to 9" or "7-9," not "7~9."

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If you wish, you may write in the first person singular or plural and use the active voice ("I observed that ..." or "We observed that ..." instead of "It was observed that ..."). Remember to check spelling. If your native language is not English, please get a native English-speaking colleague to carefully proofread your paper.

VI. Some Common Mistakes

The word "data" is plural, not singular. The subscript for the permeability of vacuum μ_0 is zero, not a lowercase letter "o." The term for residual magnetization is "remanence"; the adjective is "remanent"; do not write "remnance" or "remnant." Use the word "micrometer" instead of "micron." A graph within a graph is an "inset," not an "insert." The word "alternatively" is preferred to the word "alternately" (unless you really mean something that alternates). Use the word "whereas" instead of "while" (unless you are referring to simultaneous events). Do not use the word "essentially" to mean "approximately" or "effectively." Do not use the word "issue" as a euphemism for "problem." When compositions are not specified, separate chemical symbols by en-dashes; for example, "NiMn" indicates the intermetallic compound $Ni_{0.5}Mn_{0.5}$ whereas "Ni–Mn" indicates an alloy of some composition Ni_xMn_{1-x}.

Be aware of the different meanings of the homophones "affect" (usually a verb) and "effect" (usually a noun), "complement" and "compliment," "discreet" and "discrete," "principal" (e.g., "principal investigator") and "principle" (e.g., "principle of measurement"). Do not confuse "imply" and "infer."

Prefixes such as "non," "sub," "micro," "multi," and "ultra" are not independent words; they should be joined to the words they modify, usually without a hyphen. There is no period after the "et" in the Latin abbreviation "*et al.*" (it is also italicized). The abbreviation "i.e.," means "that is," and the abbreviation "e.g.," means "for example" (these abbreviations are not italicized).

An excellent style manual and source of information for science writers is [9]. A general IEEE style guide and an *Information for Authors* are both available at http://www.ieee.org/web/publications/authors/transjnl/index.html

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IX. CONCLUSION

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

APPENDIX

Appendixes, if needed, appear before the acknowledgment.

ACKNOWLEDGMENT

The preferred spelling of the word "acknowledgment" in American English is without an "e" after the "g." Use the singular heading even if you have many acknowledgments. Avoid expressions such as "One of us (S.B.A.) would like to thank ... ." Instead, write "F. A. Author thanks ... ." **Sponsor and financial support acknowledgments are placed in the unnumbered footnote on the first page, not here.**

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