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CONTENTS

Effect of Diffraction-Coupled Apertures on the Monopole Antenna Performance

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***Abstract* — For the first time the concept of diffraction-coupled apertures is applied to the analysis of characteristics of the cylindrical monopole antennas. The information about the spatial distribution of electromagnetic fields in the radiating region of antennas is used for studying the influence of diffraction effects on the antenna performance. The optimal radius of the round hole in the ground plane center for coupling with the coaxial feeding line is determined for all the antennas under test. Based on the results of computational modeling the small-size monopole antenna is proposed. The experimental data on the antenna prototype are in good agreement with the simulations.**

***Index Terms* — cylindrical monopole antenna, diffraction, interference, diffraction**

I. Introduction

Recently, X-band UWB communication systems are in great demand. A good candidate for this purpose is the broadband cylindrical monopole antenna [1, 2]. The advantage of this class of antennas is the ability to produce the different radiation patterns by changing the shape and size of the constituent elements of antennas [3-5], including multi-beam radiation patterns [6, 7].

State-of-the-art applications of cylindrical monopole antennas require a special study of the influence of diffraction effects on the antenna performance. Many papers are devoted to this problem [3-6, 8-13]. For example, in [13] the influence of the conducting cube size as well as the position and the length of the cylindrical monopole located on the cube surface on such parameters as the peak of the input conductance, resonant frequency and quality factor are examined. The authors have found that the greatest peak of the input conductance is archived when the monopole is located in the cube center and decreases in case of the monopole moving to a face or to a corner of the cube. At the same time, the resonant frequency of the antenna tends to move towards higher frequencies due to the influence of higher-order effects. The results of studying the influence of the ground plane size on the cylindrical monopole antenna characteristics are presented in our previous publications [3-6] and the monopole antennas with the original design of the ground plane are proposed in [3, 5, 6].

It is worth noting that the knowledge of the influence of diffraction effects on the antenna beamforming is very important not only in relation to the individual antenna but also for the antenna array composed of such elements [14, 15]. For example, in [15] the authors point out an irregular changing the angle of maximum radiation of the cylindrical monopole antenna depending on the ground plane size. Moreover, they show that a similar situation occur in the case of the antenna array.

In this paper we study in detail the diffraction effects in relation to the X-band cylindrical monopole antenna and their contribution to the performance of the antenna..

II. Antennas under test and research technique

The antennas under test consist of the vertical cylindrical monopole as a segment of the central conductor of the coaxial feeding line with a diameter of $2a$ (in our investigations $2a$=1.4mm) and the circular metal ground plane with the radius R and thickness d (in our case d=0.5mm) (Fig. 1).

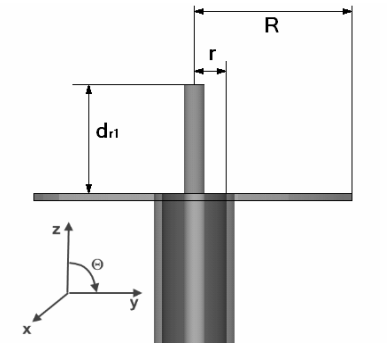

Fig. 1. Schematic view of antennas under test

In the framework of the research we focus on the two most interesting monopole heights d_{r1}, namely: quarter-wavelength ($d_{r1}=\lambda/4$) and three fourth-wavelength ($d_{r1}=3\lambda/4$) monopoles

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for the wavelength λ=30mm. The ground plane radius R varies from 7.5mm to 82.5mm with steps of 7.5mm. Furthermore, the round hole in the ground plane center for coupling with the coax has the radius r which varies from r=2.25mm, corresponding to the radius of the coaxial feeding line with the dielectric filling ε=2.04, to r=0.8mm.

The input reflection coefficient S_{11}, near-field distributions, radiation patterns and antenna bandwidth were selected by us for the analysis. The simulations were performed by using a software package for solving the scattering problems based on the standard finite difference algorithm with the "exact" absorbing conditions on the spherical artificial boundaries in free space and on the transverse artificial boundaries in the feeding line [16]. The measurements were carried out on the experimental equipment available at the LHFT [17, 18].

III. The Central Hole in the Ground Plane of Antenna

It is quite clear that the most appropriate approach for studying the edge effects caused by the diffraction of EM waves on a finite aperture is the obtaining of information on the spatial distribution of EM fields in the inductive and radiating regions of antenna. The information like that allows one to study and to analyze the dynamics of the wave packets transformation in the process of antenna beamforming. In terms of studying the diffraction phenomena, the particular importance is acquired in the most complicated case when the typical dimensions of the objects under test become comparable with the operational wavelength. With respect to the cylindrical monopole antenna there are two typical areas of the edge wave sources, namely, the ground plane edge and the edge of the round central hole in the latter. The interference of these edge waves with the initial wave packet of the monopole will result in the interference picture formation in free space. Therefore, the study of regularities in the interference pictures formation becomes the key aspect allowing one to identify the relationship of the physical parameters of antennas with their radiation pattern shape. In addition, we can assume that the interaction of such the diffraction-coupled apertures will result in the need to take into account the diffraction correction in the resonant frequency of the antenna**.**

Based on the aforementioned concept, we have been analyzed the EM field distributions in the inductive region of monopole antennas with the different ground plane radii where the influence of the ground plane size on the antenna beamforming is manifested most clearly [19]. As a result it has been determined that for the monopole antennas with $d_{r1}=\lambda/4$ two types of spatial near-field distributions depending on the ratio of the ground plane radius and the wavelength is observed. The first type of the EM field distribution has two field variations along the ground plane radius with a minimum, located at a fixed distance from the ground plane edge for antennas with the ground plane radii divisible by $\lambda/2$, and the second one looks like the circular interference picture for antennas with the ground plane radii divisible by odd number of $\lambda/4$. We have called these distributions as the "spatial wave grating". The differences like those explain the oscillating dependencies of both the resonant frequency and the elevation angle of peak directivity. In contrast to the antennas with $d_{r1}=\lambda/4$ the resonant frequency and elevation angle of peak directivity for the antennas with $d_{r1}=3\lambda/4$ are not changed virtually. The thresholds of the ground plane radii of antennas with $d_{r1}=\lambda/4$ and $d_{r1}=3\lambda/4$ corresponding to the transition from the mono-beam to multi-beam radiation pattern have been defined. Furthermore, and it has been shown that the number of beams increases when increasing the ground plane radius.

Following our concept of the diffraction-coupled apertures it is logical to assume that for each antenna configuration there is the optimal radius of the round hole in the ground plane center. To confirm this hypothesis, we performed the simulations of cylindrical monopole antennas performance with the monopole heights $d_{r1}=\lambda/4$ and $d_{r1}=3\lambda/4$ with different radii of the round hole. The minimum value of the return loss coefficient S_{11} was chosen as the criterion of the optimal radius of such a hole for each fixed-sized ground plane. Let us analyze the obtained results for the first and second groups of antennas separately taking into account the revealed above difference in the characteristics of antennas with the monopole heights $d_{r1}=\lambda/4$ and $d_{r1}=3\lambda/4$.

The comparative analysis of near-field distributions of antennas with the monopole heights $d_{r1}=\lambda/4$ and $d_{r1}=3\lambda/4$ shows that the field intensity under the ground plane of the antenna with the monopole height $d_{r1}=3\lambda/4$ is significantly less than that of the antenna with the monopole height $d_{r1}=\lambda/4$ at the same ground plane radii (Fig 2). The field intensity on the ground plane edge of the antenna with the monopole height $d_{r1}=\lambda/4$ is 5.7 times higher than that of the antenna with the monopole height $d_{r1}=3\lambda/4$. In the latter case the EM field distribution is concentrated mainly near the monopole. As a result of this, the contribution of diffraction fields to the antenna beamforming will be much smaller.

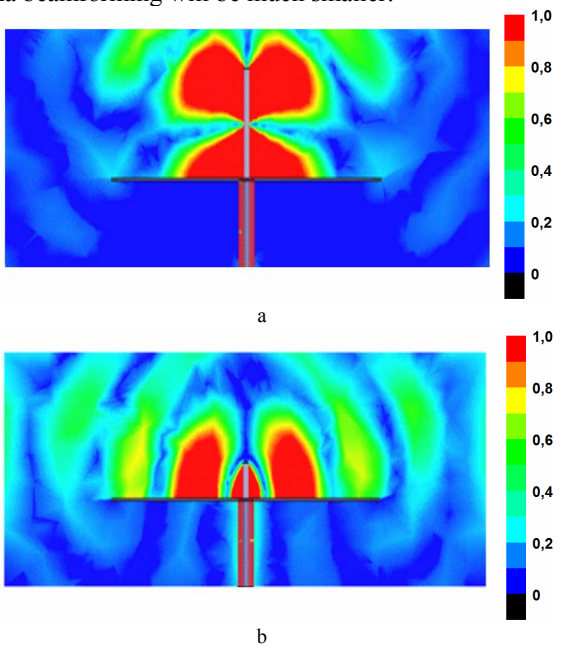
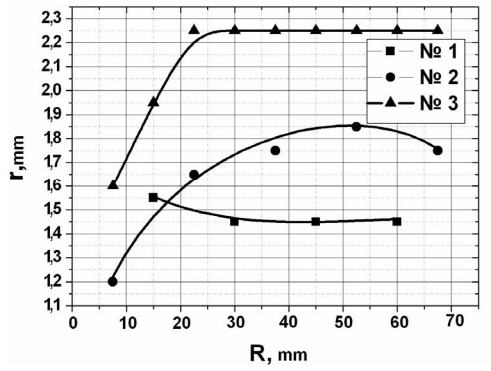
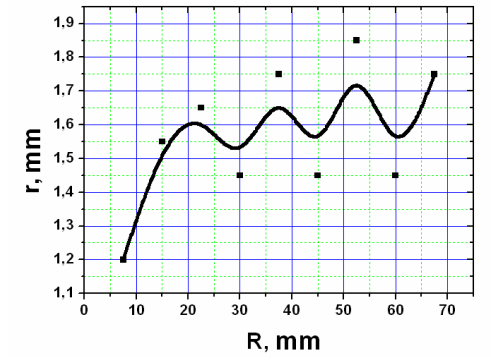


Fig. 2. Spatial near-field distribution of the electric field component ***E*** of the antenna with the monopole heights $d_{r1}=3\lambda/4$ (a) and $d_{r1}=\lambda/4$ (b) at a fixed time($R=\lambda$=30mm).

For the first group of antennas with the monopole height $d_{r1}=\lambda/4$ we observe a small change in the optimal radius of the round hole when increasing the ground plane radius (Fig. 3a, curve 1). At the same time, the optimal radius of the hole for the second group of antennas increases when the ground plane radius increases from R=7.5mm to R=52.5mm. For R>52.5mm the optimal radius of the round hole decreases (Fig. 3a, curve 2). As a result of this, the dependence of optimal round hole size on the ground plane radius for the antennas with the monopole height $d_{r1}=\lambda/4$ also demonstrates an oscillating form (Fig. 3b) similar to the aforementioned dependencies of the resonant frequency and the angle of maximum radiation [19].



a



b

Fig. 3. The optimal round hole radius depending on the ground plane radius: for antennas with $d_{r1}=\lambda/4$ (curves 1 and 2) and $d_{r1}=3\lambda/4$ (curve 3) (a); for all the antennas under study with the monopole height $d_{r1}=\lambda/4$ (b)

The analysis of the similar dependence for antennas with the monopole height $d_{r1}=3\lambda/4$ (Fig. 3, curve 3) suggests that the determination of the optimal round hole size has a meaning only for antennas with R<22.5mm, since for the antennas with R>22.5mm the optimal radius of the hole is r=2.25mm, which corresponds to the radius of the dielectric in the coaxial feeding line.

IV. The Miniature Cylindrical Monopole Antenna

Let us now consider in detail the behavior of the return loss coefficient S_{11} of the antenna with parameters R=7.5mm and $d_{r1}=\lambda/4$ when the round hole radius varies from r=2.25mm to r=0.75mm. The characteristics of antennas with the different round hole radii are shown in the Figure 4 and the Table I. By analyzing the data obtained it should be noted that the optimization of the round hole radius gives rise to a significant improvement of the antenna performance. Namely, it leads to the expansion of the antenna bandwidth and to the improvement of the antenna efficiency. In particular, the antenna with parameters R=7.5mm, $d_{r1}=\lambda/4$, and r=2.25mm has the return loss coefficient S_{11}>-10dB over the entire analyzed frequency band. For the optimal value of the round hole radius r=1.15mm the parameter S_{11} reaches the minimum value S_{11}=-32dB at the resonant frequency f=10GHz. In this case the -10dB impedance bandwidth of the antenna is equal to 16%. The further reducing the round hole size results in the increase of both the resonant frequency and the parameter S_{11} that leads to a deterioration of the antenna performance.

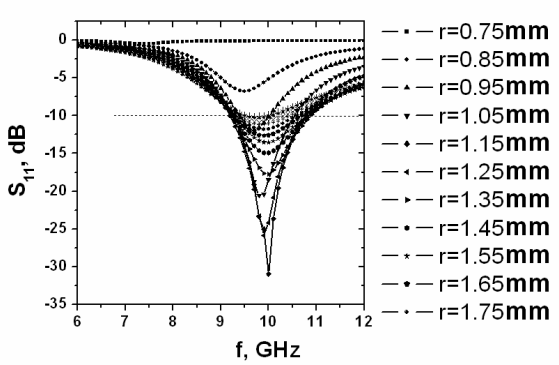


Fig. 4. Return loss coefficient S_{11} of the antenna with parameters R=7.5mm and $d_{r1}=\lambda/4$ for different round hole radii.

For the antenna with R=7.5mm and $d_{r1}=3\lambda/4$ the optimal radius of the round hole has been also determined. As one sees from the Figure 5 and the Table I, in this case the antenna efficiency also increases.

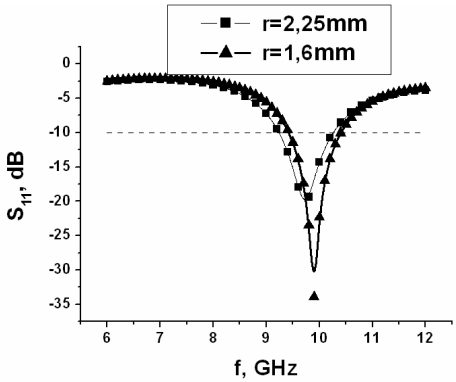


Fig. 5. Return loss coefficient S_{11} of the antenna with following parameters: R=7.5mm, $d_{r1}=3\lambda/4$, r=1.6mm, and r=2.25mm

Thus, the optimization of the round hole radius allowed us to design the miniature broadband antenna. The prototype of such the antenna has been manufactured and tested (Fig. 6, Table I).

TABLE I
CHARACTERISTICS OF THE MINITURE MONOPOLE ANTENNAS

		d_{rl}=7.5mm		d_{rl}=22.5mm	
r	2.25	1.15 theory	1.15 experiment	2.25	1.6
$f_{res.}$, GHz	9.8	10	9.96	9.7	9.9
G	-	10.53	8.9	9.28	9.42
θ_{max}	74	74	69	49	49
Δf, %(GHz)	0	16 (9.24-10.85)	15 (9.2-10.74)	10 (9.23-10.25)	10 (9.41-10.4)

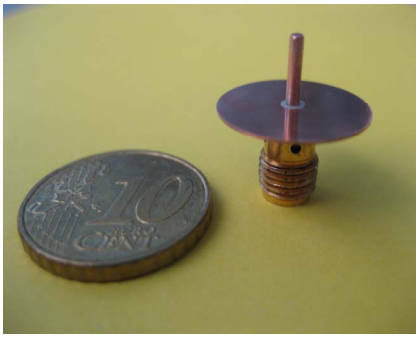
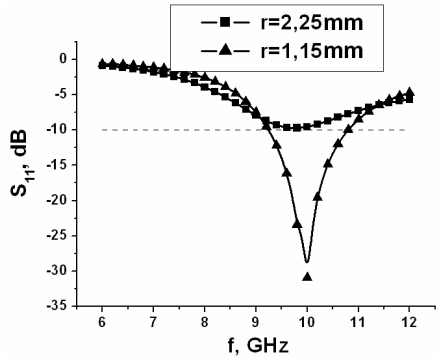
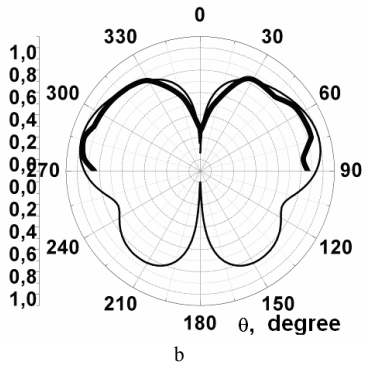


Fig. 6. Antenna prototype



a



b

Fig. 7. Return loss coefficient S_{11} of the antenna (a); measured (thick line) and simulated (thin line) radiation pattern of the antenna with parameters: d_{rl}=7.5mm, R=7.5mm, r=1.15mm (b)

The return loss coefficient S_{11} of the antenna prototype is shown in the Figure 7a along with the return loss coefficient S_{11} of the antenna having the conventional round hole radius which corresponds to the radius of the dielectric in the coaxial feeding line. The radiation pattern of the antenna is shown in the Figure 7b. As can be seen, this antenna produces mono-beam radiation pattern with the maximum radiation at $\theta=69^0$. The experimental data are in good agreement with the simulations.

V. CONCLUSION

Thus, the physical nature of oscillating dependence of the optimal round hole radius on the ground plane radius of antennas with the monopole height $d_{rl}=\lambda/4$ is explained by different conditions of the formation of spatial near-field distributions in two groups of antennas. We have established the dependence of the optimal round hole radius on the ground plane radius that indicates a validity of the approach applied by us for studying the radiation characteristics of this class of antennas in terms of diffraction-coupled apertures.

It has been determined that the variation in the round hole radius of the antenna with a fixed ground plane size results in the resonant frequency shift of the antenna and the antenna efficiency change. It has been established that for each ground plane size of the antenna with the monopole height $d_{rl}=\lambda/4$ one can choose the optimal round hole size at which the antenna performance is maximized. We have also shown that the optimization of the round hole size of the antenna with the monopole height $d_{rl}=3\lambda/4$ has a meaning only for the ground plane radii $R<3\lambda/4$.

The choice of the optimal round hole radius allowed us to offer the miniature cylindrical monopole antenna with parameters $d_{rl}=\lambda/4$, R=7.5mm, and r=1.15mm which produces a wide-angle mono-beam radiation pattern in the -10dB impedance bandwidth BW=15%. The antenna seems to be very attractive for using in wireless communications and data transmission such as WiMax.

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A Novel Wideband Circular Ring DGS Antenna Design for Wireless Communications

Rakesh Sharma, Abhishek Kandwal, and Sunil K. Khah

Abstract — **This paper introduces a novel design of a wideband defected ground circular ring antenna for wireless communication systems. The proposed antenna operates in S-band with the resonating frequency at 3.5 GHz. Designed antenna shows a wideband in the frequency range from 3.3 GHz to 3.9 GHz. The antenna is designed and tested for the calculating the parameters like impedance bandwidth, VSWR and antenna gain.**

Index Terms— **Defected ground, Wideband, Wireless, Communication**

I. Introduction

MICROSTRIP antennas have been rapidly developed in recent years and offer an attractive solution to compact, conformal and low cost designs of many wireless application systems. Microstrip patch antennas are very useful because of their advantages such as light weight, low cost, simplicity in design. Antennas are important contributors for the overall radar cross-section. Efforts have been devoted to minimize the size of microstrip antenna, with a lot of methods proposed recently, such as cutting slots on the patch, using stacked patch, and adopting the substrate with high permittivity, etc. Several techniques have been proposed to enhance the bandwidth in the state-of-the art antenna research. By using the shorting pins or shorting walls on U-shaped patch, U-slot patch, or L-probe feed patch antennas, wideband and dual band antenna with electrically small in size have been reported. Other techniques involve employing multilayer structures with parasitic patches. Moreover, some structures are engraved in the patch or ground plane to miniaturize the size of antenna [1-5]. The rapid advancement in wireless communication has attracted the interests in microstrip antennas. With the wide spread proliferation of wireless communication technology in recent years, the demand for compact, low profile and broadband antennas has increased significantly. To meet the requirement, the microstrip patch antenna has been proposed because of its low profile, light weight and low cost. Now days defected ground structure (DGS) microstrip patch antennas have been rapidly developed for multi-band and broad band in wideband communication systems [6-11].

In the present communication a novel circular ring microstrip antenna with DGS is proposed. The proposed antenna design is analyzed by simulation software CST Studio Suit and experimentally tested using vector network analyzer. Calculations are thus carried out for calculating the impedance bandwidth, voltage standing wave ratio, input impedance and radiation properties such as antenna gain and side lobe level.

II. Antenna Design

The geometry consists of a circular ring microstrip antenna with a defected ground as shown in figure (1). The circular ring antenna with DGS is designed on a commercially available glass epoxy substrate of dielectric constant 4.1 and height 1.59mm respectively. A circular ring of outer radius 23.5mm and inner radius 10mm is printed over the substrate material. Defect is introduced in the ground plane by removing metal strips of 2mm width from the ground plane below the circular ring symmetrically as shown in the figure. The antenna is fed by a coaxial probe at 13mm from the centre of the ring.

Figure 1(a,b) shows the top and bottom view of defected ground structure circular ring microstrip antenna design. The prototype of the antenna design is shown in figure (2). Figure 2(a) shows the top view and figure 2(b) shows the bottom view of the defected ground structure. The dimensions of the antenna structure are also shown in figure 2(a) and 2(b). The proposed has dimensions of (52 mm x 52 mm) with a < b, where ‘a’ is the inner radius and ‘b’ is the outer radius of the proposed circular ring defected ground antenna.

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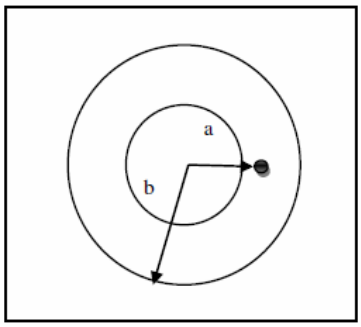

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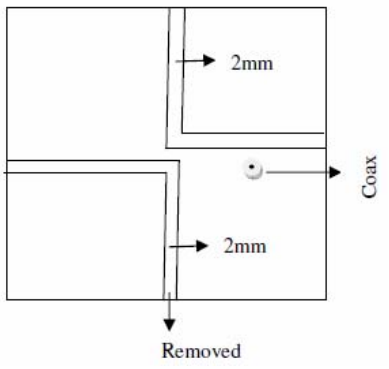

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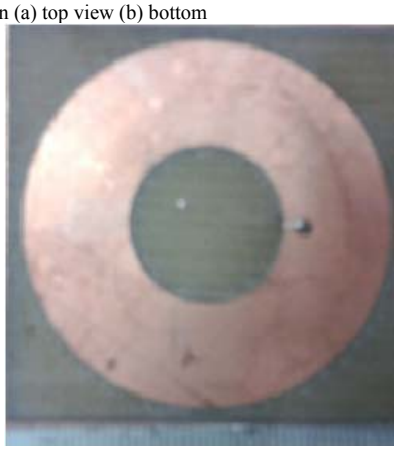
Fig. 1. Geometry of defected ground structure circular ring microstrip antenna design (a) top view (b) bottom



a

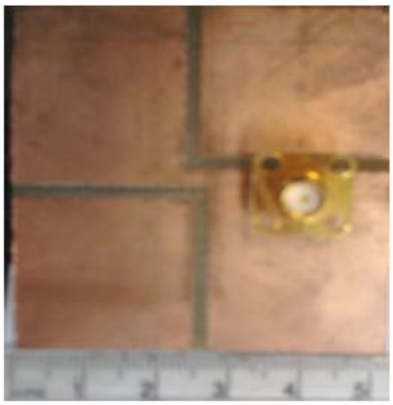


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Fig. 2. Prototype of defected ground structure circular ring microstrip antenna design (a) top view (b) bottom view

III. Results and Discussion

Results are compared for both the antenna structures, structure without defected ground plane and structure with defected ground plane. Parameters such as return loss, input impedance, bandwidth for the cases are measured, calculated and compared. Simulations are carried out using simulation software and vector network analyzer is used for experimental measurement purposes.

For the first case, when the ground plane for the designed antenna is not defected and covers whole of the substrate, the simulated and experimental graph of return loss is shown in figure 3. From the graph, we can see that the antenna shows a good return loss but not showing wide band characteristics. The antenna shows a bandwidth of about 5.8 % and 6.05 % for simulated and experimental respectively.

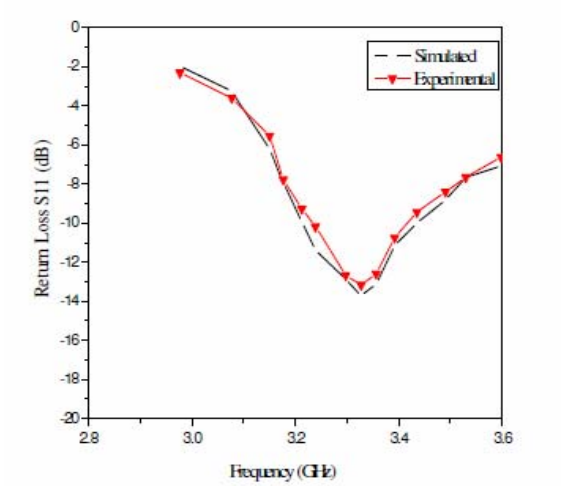

Fig. 3. Simulated and experimental return loss variation with frequency (without defect)

For the second case, when the defect in the ground plane is introduced, the antenna shows a wide band. The simulated and experimentally measured return loss is shown in figure 4.

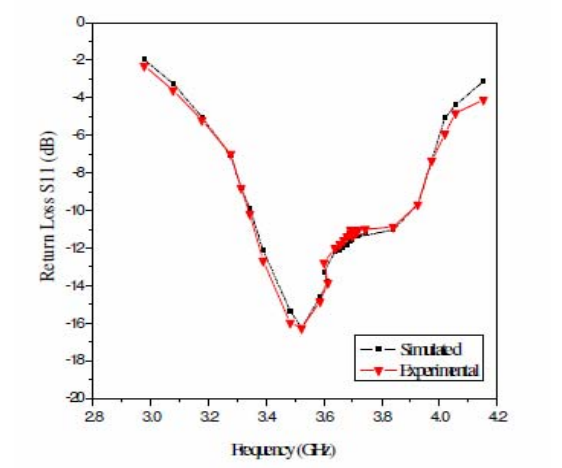

Fig. 4. Simulated and experimental return loss variation with frequency (with defect)

From this figure, we can see that the antenna shows a wideband in the frequency range of 3 – 4 GHz with good impedance matching. The antenna resonates at the frequency 3.5 GHz in the frequency range from 3.3 GHz to 3.9 GHz. The simulated impedance bandwidth calculated from the graph is 16.3 % and the experimentally measured bandwidth is about 16.6 %. The impedance curve is also shown in figure 5.

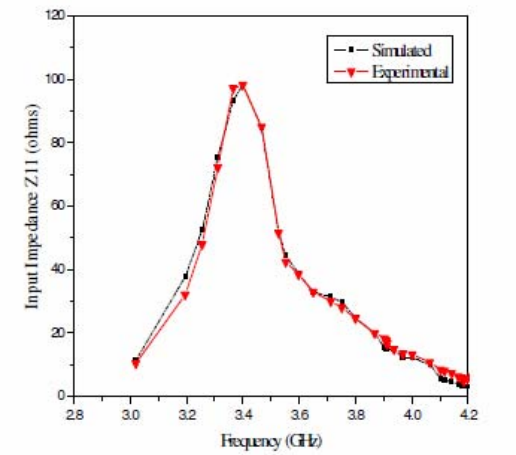

Fig. 5. Simulated and experimental input impedance variation with frequency (with defect)

A good impedance matching is obtained at the resonant frequency 3.5 GHz. Both the simulated and experimental results are in good agreement with each other.

The voltage standing wave ratio (VSWR) both simulated as well as experimentally measured is also shown in figure (6). For the frequency range 3.3 GHz to 3.9 GHz, the entire VSWR curve is ≤ 2.

The simulated radiation pattern for the defected ground antenna structure is shown in figure 6.

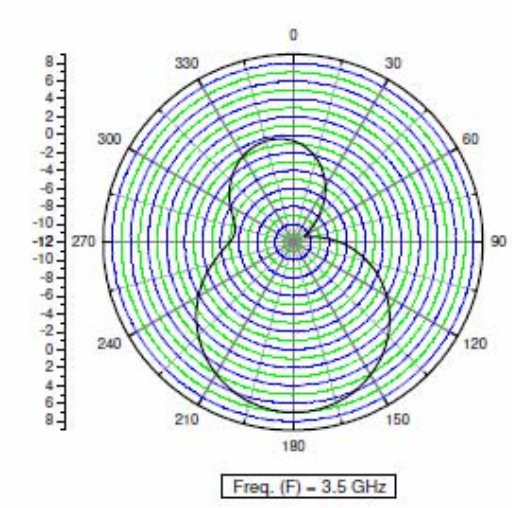

Fig. 6. Radiation pattern (with defect) for Directivity Abs (Phi = 90) between Theta/Degree vs. dBi for frequency F = 3.5 GHz

The polar plot is plotted for directivity Abs (Phi = 90) between Theta/Degree vs. dBi for the resonant frequency 3.5 GHz. in the main lobe direction 179.0 degree, the antenna gain obtained is 7.0 dBi. Within 3 dB angular width in the direction 75.3 degree, the side lobe level obtained is also reduced to a good extent of about -8.3 dB.

Therefore from the above results, we can observe that the defect in the ground plane results in the bandwidth enhancement with good radiation characteristics thereby reducing the overall size of the antenna structure. In the proposed antenna structure also, we obtain wide band with improved radiation characteristics.

IV. Conclusion

A novel defected ground microstrip ring antenna with a defected ground is presented and discussed. It is therefore observed that by introducing the defected ground plane, the characteristic properties are improved. Bandwidth of the antenna is increased to 16 % which is very good for wideband applications with a reasonable antenna gain and side lobe level. The proposed antenna is applicable for various wideband communication systems and wireless applications.

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Implementing Control Units for Linear Algorithms

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***Abstract*—Two methods are proposed for reducing the number of LUT elements in logic circuits of compositional microprogram control units with code sharing. The methods are based on usage of free resources of embedded memory blocks for representing the codes of the classes of pseudoequivalent operational linear chains. It allows reducing the number of LUTs in the block of microinstruction addressing. The example of application and results of investigations are given.**

Keywords: compositional microprogram control unit, FPGA, LUT elements, embedded memory blocks, hardware reduction.

I. Introduction

As a rule, digital systems include control units responsible for interplay of all system blocks [1]. The behaviour of a control unit (CU) is determined by a control algorithm of a digital system. Such an algorithm can be represented as a graph-scheme of algorithm (GSA) [2]. One of the very important problems connected with design of CUs is a reduction of hardware amount required for implementing the CU's logic circuit [3]. Methods used for solution of this problem depend on peculiarities of both logic elements used for implementing logic circuits and control algorithms to be interpreted [2].

Now, the field-programmable gate arrays (FPGA) [4, 5] are widely used for implementing logic circuits of digital systems. In this article, we discuss FPGA chips including look-up table (LUT) elements and embedded memory blocks (EMB) [6].

The specific of LUT is the limited number of inputs (up to 6-8). It is known that to decrease the amount of LUTs in a circuit it is necessary to decrease the numbers of both arguments and product terms in a Boolean function to be implemented. The specific of EMBs is their ability for reconfiguration in the frames of particular size. For example, the configurations 16k×1, 8k×2, 4k×4, 2k×8, 1024×18, 512×36, and 256×72 exist for typical EMBs [4, 5]. An EMB targets implementing tabular functions. It is quite possible that either some cells, or outputs, or both are not used under implementing some systems of Boolean functions. There are a lot of researches devoted to FPGA-based design of control units [7-11].

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If a control algorithm is represented by a linear GSA, then a control unit can be implemented as a compositional microprogram control unit (CMCU) [12]. The positive feature of CMCU is usage of all recourses of FPGAs (both LUTs and EMBs). It allows obtaining logic circuits with minimum possible amount of LUTs [12].

In this article, some improvements are proposed for the CMCU with code sharing. They are based on specific of both Moore finite-state-machine (FSM) [3] and EMBs. Let us point out that the proposed approach can be used for any model of CMCU [12].

II. The Model of CMCU with Code Sharing

Let a GSA Γ include a set of vertices B and a set of arcs E. Let $B = \{b_0, b_E\} \cup B_1 \cup B_2$ where b_0 is an initial vertex; b_E is a final vertex; B_1 is a set of operator vertices; B_2 is a set of conditional vertices. Operator vertices $b_m \in B_1$ include collections of microoperations $Y(b_m) \subseteq Y$, where $m = \overline{1, M}$, $M = |B_1|$, $Y = \{y_1, \ldots, y_N\}$ is a set of microoperations. Conditional vertices $b_q \in B_2$ contain elements of a set of logical conditions $X = \{x_1, \ldots, x_L\}$. Let us introduce some definitions.

Definition 1. An operational linear chain (OLC) α_g of GSA Γ is a finite vector of operator vertices $\alpha_g = \langle b_{g_1}, \ldots, b_{g_{F_g}} \rangle$ such that an arc $\langle b_{g_i}, b_{g_{i+1}} \rangle \in E$ corresponds to each pair of adjacent components of α_g $(i = \overline{1, F_g - 1})$.

Definition 2. An operator vertex $b_m \in B^g$, where $B^g \subseteq B_1$ is a set of operator vertices from the OLC α_g, is called an input of OLC α_g if there is an arc $\langle b_t, b_m \rangle \in E$, where $b_t \notin B^g$.

Definition 3. An operator vertex $b_m \in B^g$ is called an output of OLC α_g if there is an arc $\langle b_m, b_t \rangle \in E$, where $b_t \notin B^g$.

Definition 4. Operational linear chains α_i and α_j are pseudoequivalent operational linear chains (POLC) if there are arcs $\langle b_i, b_t \rangle, \langle b_j, b_t \rangle \in E$, where $b_i (b_j)$ is the output of OLC $\alpha_i (\alpha_j)$.

Definition 5. A GSA Γ is called a linear GSA if the following condition takes place:

$$\frac{M}{G} \geq 2 . \qquad (1)$$

So, a GSA Γ is a linear GSA if the number of its operator vertices at least twice exceeds the minimum number of OLCs. If condition (1) takes place, then the model of CMCU can be used [12]. Let us point out that an arbitrary OLC α_g can have up to $F_g = |B^g|$ inputs and exactly one

output, O_g. The inputs of OLC α_g form a set $I(\alpha_g) = \{I_g^1, I_g^2, ...\}$.

Let us use the approach [12] and find the partition C of the set B_1 such that $C = \{\alpha_1, \ldots, \alpha_G\}$. Let G be the minimum possible number of OLCs for the GSA Γ. Let us encode each OLC $\alpha_g \in C$ by a binary code K(α_g) having R_1 bits:

$$R_1 = \lceil \log_2 G \rceil. \quad (2)$$

Let us encode each component $b_{g_i} \in B^g$ by a binary code $K(b_{g_i})$ having R_2 bits:

$$R_2 = \lceil \log_2 (F_{\max}) \rceil. \quad (3)$$

The value of $F_{\max}$ is determined as $F_{\max} = \max(F_1, \ldots, F_G)$. Let us use the elements of a set τ for encoding of the OLCs, whereas the elements of the set T are used for encoding of the components (|τ| = R1, |T| = R2).

The encoding of the components is executed in the natural order:

$$K(b_{g_{i+1}}) = K(b_{g_i}) + 1; (g = \overline{1, G}; i = \overline{1, F_g - 1}). \quad (4)$$

Now, an operator vertex $b_m \in B^g$ corresponds to the microinstruction MI_m having the address $A(MI_m)$ determined as

$$A(MI_m) = K(\alpha_g) * K(b_{g_i}). \quad (5)$$

In (5), the sign * means the concatenation, whereas the vertex b_m corresponds to the component b_{g_i} of OLC $\alpha_g \in C$. In address $A(MI_m)$, the codes of OLC and its components are included separately (in the different bits of the address). This approach is called a code sharing.

On the base of (5), the model of CMCU with code sharing (CMCU CS) can be obtained (Fig. 1).

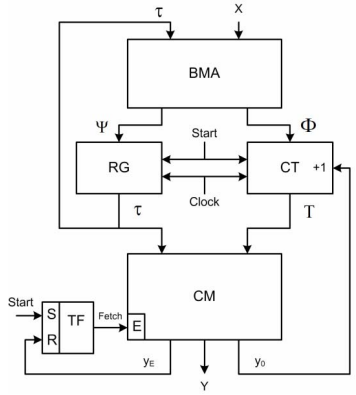


Fig. 1. Structure diagram of CMCU with code sharing

In the CMCU CS, a block of microinstruction addressing (BMA) implements systems of input memory functions for flip-flops of a register RG and a counter CT:

$$\Psi = \Psi(\tau, X); \quad \Phi = \Phi(\tau, X). \quad (6)$$

This CMCU operates in the following manner. If Start = 1, then the process begins and zero codes are loaded into both RG and CT. At the same time, a flip-flop of fetching (TF) is set up. Now, there is Fetch = 1, and microinstructions can be fetched out the control memory (CM). Let in the instant t the contents of RG and CT form some address $A(MI_m)$ corresponding to the vertex $b_m \in B^g$. This microinstruction is fetched out the CM. If $b_m \neq O_g$, then a variable y_0 is generated causing incrementing the counter CT. It provides the mode of addressing (4). In the instant t+1the next microinstruction is fetched; it still corresponds to some component of the OLC α_g. If the output O_g is reached, then the variable y_0 is not generated. It allows loading both RG and CT from the outputs of BMA. Now, a transition is executed between the output of OLC α_g and an input of some other OLC (maybe, the same OLC α_g). The process is terminated when a variable y_E is generated. It corresponds to the situation $\langle O_g, b_E \rangle \in E$.

The LUTs and latches are used for implementing logic circuits of BMA, RG, CT and TF, whereas the EMBs are used for implementing the control memory CM. If EMBs have some free recourses (cells, outputs or both), then we propose to use them for decreasing the number of LUT elements in the circuit of BMA.

III. The Main Idea of Proposed Method

As shown in [12], an OLC $\alpha_g \in C$ is an equivalent of some state of Moore FSM. So, pseudoequivalent OLCs correspond to the pseudoequivalent states of Moore FSM [3]. It means that the table of transitions of CMCU CS can be reduced by replacing the pseudoequivalent OLCs by the corresponding class of POLC. It allows decreasing the number of product terms in the functions (6) and, therefore, the reduction of the amount of LUTs in the circuit of BMA. We proposed to keep the codes of classes of POLC in free recourses of EMBs. There are two possible approaches for usage of EMBs:

1. If there are enough free outputs, then the codes of classes of POLC can be included as a separate field in the microinstruction format. Let us call this approach as the expansion of microinstruction format (EMF-approach).
2. If there are enough free cells, then an additional microinstruction with the class code can be included into each OLC of a particular class. Let us call this approach as the modification of OLC (MOLC-approach).

Let us form a set $C_1 \subseteq C$. Let $\alpha_g \in C_1$ if $\langle O_g, b_E \rangle \notin E$. Let us find a partition $\Pi_C = \{B_1, \ldots, B_I\}$ of the set C_1 by the classes of POLCs. It can be done in a trivial way, using the definition 4 from the section 2. Let us encode each class $B_I \in \Pi_C$ by a binary code $K(B_i)$ using R_3 bits, where:

$$R_3 = \lceil \log_2 I \rceil. \quad (7)$$

Let us use the variables $z_r \in Z$ for such an encoding, where $|Z| = R_3$. In this case the system (6) can be transformed in the following way:

$$\Psi = \Psi(Z, X);$$
$$\Phi = \Phi(Z, X). \quad (8)$$

In the case of CMCU CS, the control memory should include M_0 cells. Each of these cells has t_0 bits:

$$M_0 = 2^{R_1+R_2}, \quad (9)$$
$$t_0 = \underline{N} + 2. \quad (10)$$

The value 2 is added to N to take into account the variables y_0 and y_E.

The FPGA chip includes EMBs having V_0 cells if the number of outputs $t_F = 1$. Let us point out that the value of t_F can be taken from some set of fixed values $O_F = \{1, 2, 4, 8, 9, 16, 18, 32, 36, 72\}$. Let us choose the value of $t_F^0 \in O_F$ such that the difference Δt is minimal:

$$\Delta t = t_F^0 - t_0 - R_3 \geq 0. \quad (11)$$

Now, if the condition

$$(V_0 / t_F^0) \geq M_0 \quad (12)$$

takes place, then the EMF-approach can be used. It results in the CMCU FCS (Fig. 2).

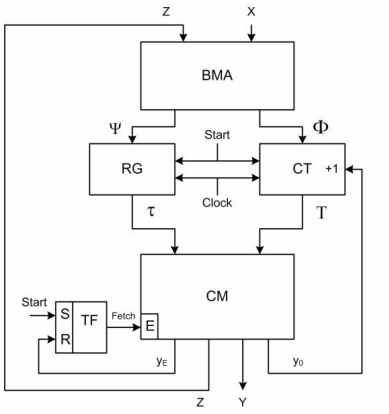


Fig. 2. Structure diagram of CMCU FCS

In the case of MOLC-approach, the number of required memory cells is determined as

$$M_1 = M + G. \quad (13)$$

Let the following condition take place for any OLC $\alpha_g \in C_1$:

$$F_g \leq 2^{R_2} - 1. \quad (14)$$

In this case, the introduction of additional microinstructions does not increase the value of R_2 in comparison with (3). Now, the value of t_F^0 is chosen from the following condition

$$\Delta t = t_F^0 - t_0 \geq 0;$$
$$\Delta t \rightarrow \min. \quad (15)$$

If condition (14) takes place, then the MOLC-approach can be used leading to the CMCU MCS (Fig. 3).

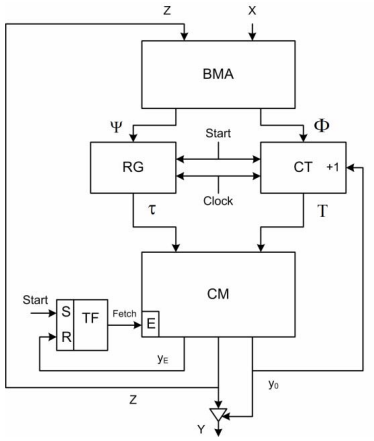


Fig. 3. Structure diagram of CMCU MCS

Let us point out that the EMF-approach is more preferable. It does not require additional (idle) cycles of CMCU. So, it is necessary to start from the model of CMCU FCS. If this model cannot be used, then the model of CMCU MCS should be tried. Let us discuss the case when both models can be used and, moreover, only one EMB is enough for implementing the control memory. In other cases, the proposed methods need some modifications. The modifications are not complex, and, because of it, they are beyond the scope of this article.

The proposed design methods include the following steps:

1. Constructing the sets C, C_1, Π_C for a given GSA Γ.
2. Encoding of OLC $\alpha_g \in C$ and their components.
3. Encoding of the classes $B_i \in \Pi_C$.
4. Constructing the content of control memory.
5. Constructing the table of transitions of CMCU and finding the system (8).
6. Implementing the logic circuit using given FPGA chip.

The step 1 is executed using the methods from [12].As a result, the number G of OLC $\alpha_g \in C$ is minimal. The partition Π_C is formed using the definition 4.

The encoding of OLC should be executed in a way minimizing the number of terms in (8). The well-known methods [1] can be used to solve this problem. The components of OLC $\alpha_g \in C$ are encoded in a trivial way. The first component of any OLC has the code whose decimal equivalent is equal to zero. The codes of the second components are equal to 1, the third – to 2 and so on. This style of encoding satisfies to (4). The codes of classes do not affect the number o LUTs in the circuit of BMA.

The content of CM is represented by the table having the fields $A(MI_m)$, $Y(b_m)$, y_0, y_E, $K(B_i)$. In the case of CMCU FCS, the fields $Y(b_m)$ and $K(B_i)$ require different bits. In the case of CMCU MCS, these fields share the same bits of EMB. The number of required bits is determined as max (N+2; R_3).

To construct the table of CM, it is necessary to transform the initial GSA Γ [12]. If a vertex $b_m \in B^g$ is not the output of OLC $\alpha_g \in C$, then the variable y_0 is introduced into this

vertex. If $\langle b_m, b_E\rangle \in E$, then the variable y_E is introduced into the vertex $b_m \in B_1$.

The table of transitions is constructed on the base of generalized formulae of transitions [12]:

$$B_i \to \bigvee_{h=1}^{H_i} X_h b_m; (i = \overline{1, I}). \quad (16)$$

In (16), X_h is a conjunction of logical conditions determining the transition from the output of any OLC $\alpha_g \in B_i$ to the operator vertex b_m; H_i is the number of transitions from this output. The system (16) leads to the table of transitions having the following columns: B_i, $K(B_i)$, b_m, $A(MI_m)$, X_h, Ψ_h, Φ_h, h. Here $\Psi_h \subseteq \Psi$ is a set of input memory functions for the RG; $\Phi_h \subseteq \Phi$ is a set of input memory functions for the CT; h is a number of transitions. The system (8) is constructed as the following:

$$D_r = \bigvee_{h=1}^{H} C_{rh} B_h X_h; (r = \overline{1, R_2 + R_3}). \quad (17)$$

In (17), C_{rh} is the Boolean variable equal to 1 iff the function D_r is written in the h-th row of the table, B_h is a conjunction of variables $z_r \in Z$ corresponding the code $K(B_i)$ for the h-th row of the table $(h = \overline{1, H})$.

The last step is reduced to implementation of the logic circuit of CMCU using some standard tools [4, 5].

IV. An example of application of proposed methods

Let some GSA Γ_1 include $M = 17$ operator vertices. Let these vertices form the set $C = \{\alpha_1, \ldots, \alpha_8\}$ where $\alpha_1 = \langle b_1, b_2\rangle$, $\alpha_2 = \langle b_3, b_4, b_5\rangle$, $\alpha_3 = \langle b_6, b_7\rangle$, $\alpha_4 = \langle b_8, b_9, b_{10}\rangle$, $\alpha_5 = \langle b_{11}, b_{12}\rangle$, $\alpha_6 = \langle b_{13}, b_{14}\rangle$, $\alpha_7 = \langle b_{15}, b_{16}\rangle$ and $\alpha_8 = \langle b_{17}\rangle$. It means $G = 8$, condition (1) takes place and the model of CMCU can be used.

Let $\alpha_8 \notin C_1$, $L = 4$, $N = 6$ and $\Pi_C = \{B_1, \ldots, B_4\}$, where $B_1 = \{\alpha_1, \alpha_6\}$, $B_2 = \{\alpha_2, \alpha_3, \alpha_5\}$, $B_3 = \{\alpha_4\}$, $B_4 = \{\alpha_7\}$.Because there is $G = 8$, then $R_1 = 3$ and $\tau = \{\tau_1, \tau_2, \tau_3\}$. It can be found that $F_{\max} = 3$; it means that $R_2 = 2$ and $T = \{T_1, T_2\}$. Let us encode the OLC $\alpha_g \in C$ in a trivial way: $K(\alpha_1) = 000$, $K(\alpha_2) = 001$, …, $K(\alpha_8) = 111$. The first components at any OLC $\alpha_g \in C$ have the code 00, the second components have the code 01, the third components have the code 10 and the fourth components have the code 11. Let us point out that in the discussed example the fourth components are added into some OLCs of CMCU MCS.

The addresses of microinstructions can be found from Table I. In this table, the symbols $(b_{18}) - (b_{24})$ denote additional vertices introduced for CMCU MCS.

Let the following system of generalized formulae of transitions can be obtained after analysis of the GSA Γ_1:

$$B_1 \to x_1 b_3 \vee \overline{x_1} x_2 b_8 \vee \overline{x_1}\,\overline{x_2} b_6;\quad B_2 \to x_4 b_{15} \vee \overline{x_4} b_{17};$$
$$B_3 \to x_3 b_{11} \vee \overline{x_3} b_{13};\qquad B_4 \to x_5. \quad (18)$$

TABLE I
ADDRESSES OF MICROINSTRUCTIONS

OLC $\tau_3\tau_2\tau_1$ / T_2T_1	α_1 000	α_2 001	α_3 010	α_4 011	α_5 100	α_6 101	α_7 110	α_8 111
00	b_1	b_3	b_6	b_8	b_{11}	b_{13}	b_{15}	(b_{17})
01	b_2	b_4	b_7	b_9	b_{12}	b_{14}	b_{16}	–
10	(b_{18})	b_5	(b_{20})	b_{10}	(b_{22})	(b_{23})	(b_{24})	–
11	–	(b_{19})	–	(b_{21})	–	–	–	–

Let us encode the classes $B_i \in \Pi_C$ in a trivial way: $K(B_1) = 00$, ..., $K(B_4) = 11$. Using these codes and the system (18), the table of transitions can be constructed (Table II).

TABLE II
TABLE OF TRANSITIONS OF CMCU

B_i	$K(B_i)$	b_m	$A(MI_m)$	X_h	Ψ_h	Φ_h	h
B_1	00	b_3	00100	x_1	D_1	–	1
		b_8	01100	$\overline{x_1} x_2$	$D_2\, D_1$	–	2
		b_6	01000	$\overline{x_1}\,\overline{x_2}$	D_2	–	3
B_2	01	b_{15}	11000	x_4	$D_3\, D_2$	–	4
		b_{17}	11100	$\overline{x_4}$	$D_3\, D_2\, D_1$	–	5
B_3	10	b_{11}	10000	x_3	D_3	–	6
		b_{13}	10100	$\overline{x_3}$	$D_3\, D_1$	–	7
B_4	11	b_5	00110	1	D_1	D_4	8

The addresses of microinstructions A(IMm) are taken from Table 1 using the expression (5). For example, $b_5 \in B^2$ and $K(\alpha_2) = 001$. Therefore, $A(MI_5) = K(\alpha_2)^* K(b_5) = 00110$.

Table 2 is the base for constructing the system (8). In the discussed case, this system is the following one:

$$D_1 = F_1 \vee F_2 \vee F_5 \vee F_7 \vee F_8;\quad D_2 = F_2 \vee F_3 \vee F_4 \vee F_5;$$
$$D_3 = F_4 \vee F_5 \vee F_6 \vee F_7;\qquad D_4 = F_8, \quad (19)$$

where $F_1 = \overline{z_1 z_2 x_1}$, $F_2 = \overline{z_1 z_2 x_1 x_2}$, $F_3 = \overline{z_1 z_2 x_1 x_2}$, …, $F_8 = z_1 z_2$.

Let $Y(b_3) = \{y_1, y_3, y_0\}$, $Y(b_4) = \{y_4, y_0\}$, $Y(b_5) = \{y_5\}$, $Y(b_6) = \{y_2, y_0\}$, $Y(b_7) = \{y_3, y_6\}$. Using addresses from Table I, the following fragment of content of control memory can be created for CMCU FCS (Table III).

Because the relation $\alpha_2 \in B_2$ takes place, the code $K(B_2) = 01$ is placed into the cell with address 00110. This cell corresponds to the output of OLC α_2. This very code is placed into the cell corresponding to the output of OLC α_3.

In the case of CMCU MFS, the second and the third bits of microinstruction are used either as microoperations y_1, y_2 or variables z_2, z_1 (Table IV).

TABLE III
PART OF CONTROL MEMORY FOR CMCU FCS

Address					Microinstruction										b_m	α_i
τ_3	τ_2	τ_1	T_2	T_1	y_E	y_1	y_2	y_3	y_4	y_5	y_6	y_0	z_2	z_1		
0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	b_3	
0	0	1	0	1	0	0	0	0	1	0	0	1	0	0	b_4	α_2
0	0	1	1	0	0	0	0	0	0	1	0	0	**0**	**1**	b_5	
0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	–	
0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	b_6	
0	1	0	0	1	0	0	0	1	0	0	1	0	**0**	**1**	b_7	α_3
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	–	
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	–	

TABLE IV
PART OF CONTROL MEMORY FOR CMCU MCS

Address					Microinstruction								b_m	α_i
τ_3	τ_2	τ_1	T_2	T_1	y_E	y_1 z_2	y_2 z_1	y_3	y_4	y_5	y_6	y_0		
0	0	1	0	0	0	1	0	1	0	0	0	1	b_3	
0	0	1	0	1	0	0	0	0	1	0	0	1	b_4	α_2
0	0	1	1	0	0	0	0	0	0	1	0	0	b_5	
0	0	1	1	1	0	**0**	**1**	0	0	0	0	0	b_{19}	
0	1	0	0	0	0	0	1	0	0	0	0	1	b_6	
0	1	0	0	1	0	0	0	1	0	0	1	0	b_7	α_3
0	1	0	1	0	0	**0**	**1**	0	0	0	0	0	b_{20}	
0	1	0	1	1	0	0	0	0	0	0	0	0	–	

We do not show the logic circuits of these CMCUs. But we developed CAD tools allowing synthesis of proposed models of CMCU. Our CAD tools use Xilinx ISE WebPack to produce a final implementation.

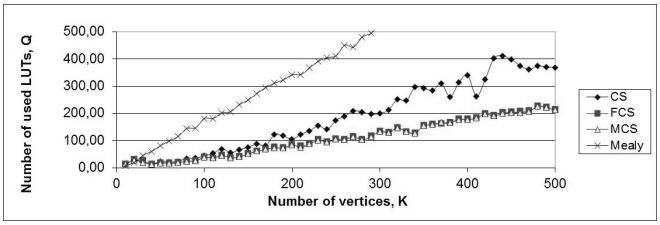
V. EXPERIMENTAL RESULTS

Our CAD system is based on the following principles. An initial GSA is represented in the XML format. One of its blocks generates VHDL-description of a given model of CMCU, together with data using for programming EMBs. This information is transferred into the system Xilinx ISE WebPack. Next, the implementation of a logic circuit is executed. The initial GSAs are generated by a special generator, which is the part of CAD tools:

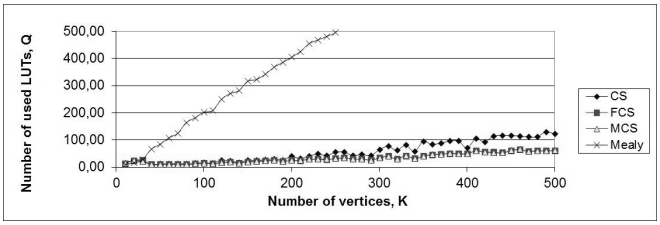
- the number of vertices K is changed from 10 to 500;
- the part of operator vertices is changed from 50 % to 90 %;
- the number of microoperations $N = 15$;
- the number of logical conditions $L = 5$.

For each GSA, the following control units were implemented: CMCU with code sharing, CMCU FCS, CMCU MCS, and Mealy FSM. The experimental results are shown on diagrams. Each point on the diagrams is an average result obtained for five different GSAs with similar parameters.

The numbers of LUTs required for implementing logic circuits of different control units are shown on Fig. 4. The results for GSAs with 70 % of operator vertices are shown on Fig. 4, a. The results for GSAs with 90 % of operator vertices are shown on Fig. 4, b. Analysis of Fig. 4 shows that the proposed models of CMCU require fewer amounts of LUTs than both Mealy FSM and the base model of CMCU CS. Moreover, the growth in the number of operator vertices leads to increasing the hardware amount for Mealy FSM. But it has quite opposite effect in the cases of CMCU.



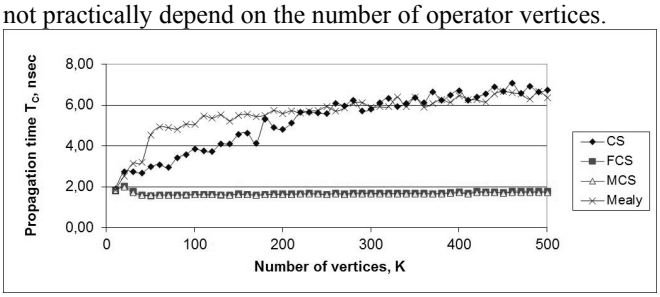
a



b

Fig. 4. Number of LUT elements in logic circuits of control units

The temporal characteristics of different control units are shown in Fig. 5. As in previous case, results for GSAs with 70 % of operator vertices are shown in Fig. 5, a. Results for GSAs with 90 % of operator vertices are shown in Fig. 5, b. Both diagrams show minimal possible propagation time T_C for the control units under investigation. The analysis if Fig. 5 shows that the proposed models provide higher performance in comparison with both Mealy FSM and CMCU CS. It is interesting that the propagation time does not practically depend on the number of operator vertices.



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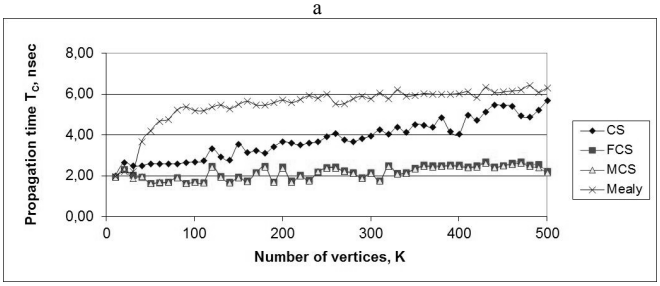

b

Fig. 5. Minimal propagation time for different control units

So, if the CMCU FCS and MCS require the same amount of EMBs, their characteristics (number of LUT elements and propagation time) are practically identical. Obviously, a control algorithm's execution requires more cycles in CMCU MCS than in the case of equivalent CMCU FCS. It is connected with existence of additional microinstructions in the control memory of CMCU MCS. So, if there are such conditions that both proposed models can be used, then the model of CMCU FCS is more preferable.

Let us point out that results of investigation are obtained for the FPGA Spartan-3 by Xilinx. If other chips are used, the results can be different. But the tendency remains.

VI. Conclusion

As the results of investigations show, the proposed methods allow decreasing the hardware amount (in average) to 40% in comparison with known design methods.

One of the results of investigation is obtaining the formula showing the hardware amount required for implementing CMCU with code sharing and proposed modifications. Let us point out that this formula is correct for FPGA chips having LUT elements with four inputs (for example, for Spartan-3 family by Xilinx). The formula is the following:

$$Q = (-0.026P_1^2 + 2.56P_1 - 10.11) \cdot K \qquad (20)$$

In (20), Q is the number of LUTs in a logic circuit, K is the number of vertices in the GSA Γ, P_1 is a part of operator vertices in a GSA Γ ($0.5 \le P_1 \le 1$). Let us point out that the expression (18) is correct for $L = 5$. If similar formulae include L as a variable, then they can be used for preliminary estimation of hardware amount in the case of an arbitrary GSA.

The time Clock for proposed models is in the interval [1.7 nsec; 2.5 nsec]. As our investigations show, this interval is equal to [5 nsec; 6 nsec] for Mealy FSM. Moreover, this characteristic for CMCU depends only on the type of FPGA. In the case of Mealy FSM, delays increase with increasing the numbers of vertices in a control algorithm.

So, the proposed models of control units allow designing logic circuits with better hardware and timing characteristics in comparison with known models. Let us point out that they can be used only if a control algorithm is represented by a linear graph-scheme of algorithm.

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Organization of Control Units with Operational Addressing

Barkalov A. A., Babakov R. M., Titarenko L. A.

Abstract — **The using of operational addressing unit as the block of control unit is proposed. The new structure model of Moore finite-state machine with reduced hardware amount is developed. The generalized structure of operational addressing unit is suggested. An example of synthesis process for Moore finite-state machine with operational addressing unit is given. The analytical researches of proposed structure of control unit are executed.**

Index Terms — **control unit, graph-scheme of algorithm, operational addressing, hardware amount, operation of transition**

I. Introduction

A control unit is one of the most important blocks of a vast majority of digital systems [1]. It can be organized as a finite-state-machine (FSM) where the input memory functions are represented by a system of Boolean equations [2]. As a rule, the hardware amount in the FSM's logic circuit increases with the growth for the number of vertices and their interconnections in a control algorithm to be implemented [3].

The system of input memory functions is implemented as an irregular circuit. As a rule, it does not include standard functional blocks such as adders, decoders and so on [4]. Because of it, the process of control unit's design causes many problems for designers of digital systems [1].

Now, the field programmable logic devices such as CPLD or FPGA are widely used for implementing logic circuits of digital systems [5]. There is a contradiction between the abilities of design libraries of CAD tools and the level of their usage in the design process of FSM's circuits. The libraries include adders, shifters, multiplexors and other blocks up to microprocessor [6, 7]. On the other hand, only low-level elements are used for designing control units. It could be either look-up table (LUT) elements and embedded memory blocks (EMB) in the case of FPGAs or the macrocells based on programmable array logic elements in the case of CPLDs [4]. In this article, we propose a new approach allowing overcoming the gap between the content of CAD libraries and the current usage of primitive elements for designing FSM's circuits.

In many practical cases, the FPGA-based Moore FSM is used [8]. There are a lot of methods using for minimizing the number of LUTs in an FSM logic circuit. The most efficient methods are connected with using multiplexers and EMBs for implementing the FSM logic circuits [9 - 11]. Application of these methods leads to decreasing for both the number of interconnections and power consuming. But it is quite possible situations when all resources of EMBs for a given chip are used for implementing other parts of a particular project. In these situations, it is impossible to use the EMB-based design methods for implementing control units. So, the problem of decreasing for the number of LUTs in the FSM logic circuit is still very important.

In this article, we propose the method of operational addressing which allows implementing the input memory functions using standard functional devices such as adders, shifters and so on. Our approach is based on implementing the input memory functions using some arithmetical and logical operations [12].

II. Proposed Organization of Control Unit

The main task of a control unit is the generation of a sequence of microoperations to control the actions of a system data-path [1]. This sequence is determined by both a control algorithm to be implemented and values of logical conditions to be checked. Let us use the term "operational automaton" for the system data-path. The operational automaton (OA) executes primitive operations (microoperations) using such blocks as adders, subtractors, multipliers, shifters and so on [13]. Let us name these blocks as "operational blocks". There are no operational blocks in control units. The only exception is the application of counters in the microprogram control units [14]. In the case of FSM, the data processing is executed with help of logical operations. Sometimes, tabular functions are executed using some memory blocks. For example, the system of microoperations of the Moore FSM can be implemented using PROMs [4].

Let us consider a control unit represented by the Moore FSM (Fig. 1).

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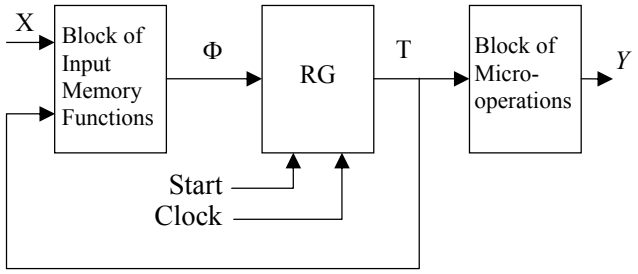

Fig. 1. Structure diagram of Moore FSM

In this model, the block of input memory functions (BIMF) implements the system of input memory functions:

$$\Phi = \Phi(T, X). \quad (1)$$

In the system (1), the set $T=\{T_1, ..., T_R\}$ is a set of state variables used for the state assignment, the set $X=\{x_1, ..., x_L\}$ is a set of logical conditions [3]. The set of internal states A includes M elements. It is known [3] that the minimum number of bits for state assignment is determined by the following equation:

$$R = \lceil log_2 M \rceil. \quad (2)$$

The block of microoperations (BMO) implements the system of microoperations $Y=\{y_1, ..., y_N\}$:

$$Y = Y(T). \quad (3)$$

The system (3) can be implemented using, for example, PROM, whereas the system (1) requires logic elements for its implementing. The logic elements can be either gates, or macrocells of CPLD, or LUT elements of FPGA. The circuit of BIMF is irregular and its implementation causes the most of design problems. To diminish the number of logic elements in the BIMF very complex methods of functional decomposition are used [15-17], as well as different methods of state assignment [18-20]. When large library elements are used, these problems are solved before the implementing proposed FSM with operational addressing (OA).

Let us point out that the pulse *Start* is used to load the code of initial state into register RG. The pulse *Clock* is used for changing the content of RG (it is a code of a current state $a_m \in A$).

Let us transform the Moore FSM (Fig. 1) in the following way:

1. Each line of a table representing BMO includes two fields. The field FY contains information about microoperations to be executed in the state $a_m \in A$. The field FO contains information about operations to be executed using $K(a_m)$ as an operand to obtain the code of the next state $a_s \in A$.

2. The BIMF is represented as an operational addressing unit (OAU). In each cycle of FSM's operation, the OAU executes one of S operations $f_s \in F=\{f_1, ..., f_S\}$. This operation uses both the code of current state and values of logical conditions to calculate the code of the next state.

Let us use the term "an FSM with operational addressing" for the resulting FSM shown in Fig. 2.

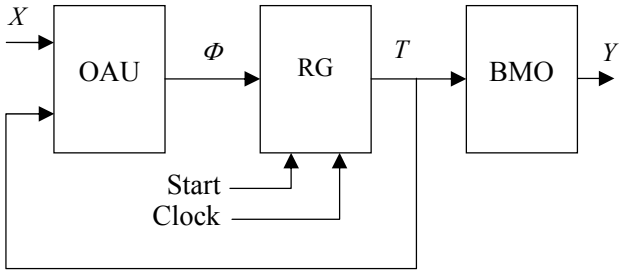

Fig. 2. Structure diagram of FSM with operational addressing

The proposed FSM with OA operates in the following order. If there is *Start* = 1, then the zero code is loaded into the register RG. It corresponds to the beginning of the operation. In each cycle the register contains a code of current state $a_m \in A$. The BMO generates microoperations $y_n \in Y(a_m)$, where $Y(a_m) \subseteq Y$ is a set of microoperations generated in the state $a_m \in A$. At the same time, the code $K(a_m)$ determines the variables from the field FY. These variables enter the input of OAU and causes execution of some arithmetical or logic operations. As a result, new values of input memory functions $D_r \in \Phi$ are generated to load the code of the next state $a_s \in A$ into RG.

The very important specific feature of OAU is a limited number of operational blocks in use. It is connected with the fact that the number of operations $f_s \in F$ is limited, too. For example, the following operations can be executed: the addition, the subtraction, the logic shift, the bit-wise inversion. The operations can be complex. It means they can be represented by a sequence of some asynchronous operations (for example, "shift → plus constant → negation → minus constant"). The set of operations F is constructed by the designer on the base of analysis of a control algorithm to be implemented. Let a control algorithm be represented by a graph-scheme of algorithm (GSA) [1].

III. General Synthesis Methods for FSM with Operational Addressing

Let us name the proposed approach for calculating codes of states the operational addressing. In this article, we propose two general methods for synthesis of the FSM with OA. In the case of operational addressing, each transition for a particular FSM is executed using only operations $f_s \in F$:

$$K(a^{t+1}) = f_s^t(K(a^t), X^t). \quad (4)$$

In (4), the symbol t stands for time (t=0, 1, 2, …), $a^t \in A$ is a current state, a^{t+1} is the next state (state of transition), f_s^t is some operation, determined by the field FO, X^t is a vector of logical conditions in the instant t, $X^t = <x_1^t, x_2^t, ...>$, $x_l^t \in \{0, 1\}$.

It follows from (4) that the state codes cannot be assigned in an arbitrary manner. They should "obey" to the operations $f_s \in F$. Therefore, two different approaches are possible for state assignment. In the first approach, the state codes are

determined after the choice of operations $f_s \in F$. In the second approach, the operations $f_s \in F$ are determined after executing the state assignment. In both cases, a state code should be treated as a number (arithmetical value) used in the operations $f_s \in F$. At the same time, this number can be considered as a binary code used for addressing BMO.

So, two methods are possible for synthesis of FSM with OA. Let us denote them as M_1 and M_2 respectively.

The proposed method M_1 includes the following steps:

1. Constructing the set of operations F.
2. Executing the state assignment on the base of operations $f_s \in F$.
3. Constructing content of the BMO.
4. Implementing logic circuit using given logic elements.

The proposed method M_2 includes the following steps:

1. Executing the state assignment.
2. Constructing the set of operations F on the base of state codes.
3. Constructing content of the BMO.
4. Implementing logic circuit using given logic elements.

Let us point out the most important issue of the proposed approach. The logic circuit of OAU is synthesized using standard operational blocks implementing operations $f_s \in F$. It differ our approach from the classical one, where the logic circuit of BIMF is implemented using a system of Boolean functions. In the case of Moore FSM (Fig. 1), each transition corresponds to a unique product term. In the case of FSM with operational addressing, each operation from F can determine a lot of transitions. As a rule, the more transitions some FSM has, the more hardware its logic circuit needs. But the FSM with operational addressing does not obey this rule.

If each operation $f_s \in F$ is used for calculation more than one state code, then the hardware amount in the logic circuit of FSM with operational addressing can be less than in the logic circuit of Moore FSM. Moreover, the standard operational blocks are optimized on the transistor level [4]. It means that the hardware amount in the final circuit is optimal, too. Besides, the performance of FSM with OA can be higher in comparison with a multilevel circuit of BIFM.

To minimize the hardware amount of OAU, the authors recommend using the following rules:

1. The set of operations F should be minimally sufficient for implementing all possible transitions between the FSM states.
2. Functional blocks should be taken from the standard library elements. They should have the minimum possible number of bits.

As a conclusion, we can say that the using operational addressing leads to representing an FSM as a composition of an operational automaton, a register and a memory block. The proper choice of operations $f_s \in F$ provides a rigid connection between the FSM with OA and an initial control algorithm.

IV. Example of Synthesis

Let us discuss an example of synthesis for FSM with OA. In this example, we only show the basic design principles. Because the example is small, it cannot illustrate possible gains in both hardware and performance. Of course, we cannot show a big example due to the lack of the article space.

Let the control algorithm be represented by a GSA Γ_1 (Fig. 3).

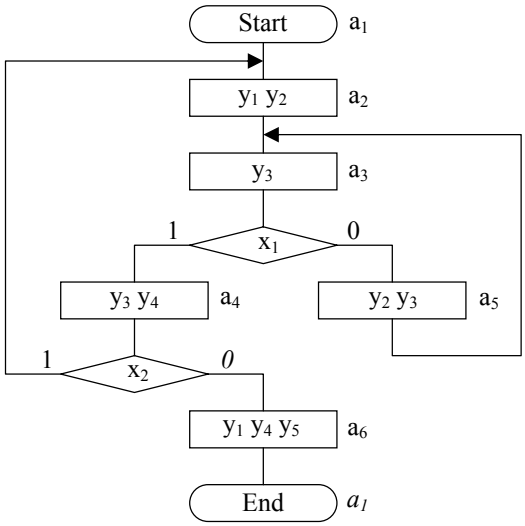

Fig. 3. Initial GSA Γ_1

Let us use the first design method and start from choosing the system F. Let us use the symbol a^t as a code of the state $a_m \in A$ in the instant t. Let it be the set $F=\{f_1, f_2, f_3\}$ and let the functions $f_s \in F$ have the following meaning:

1) The function f_1 corresponds to direct unconditional jump:

$$f_1(a^t) = a^t - k. \quad (5)$$

In (5), the symbol k stands for some constant.

2) The function f_2 executes the conditional jump. It has two outcomes depended on the value of a logical condition to be checked:

$$f_2(a^t, x^t) = \begin{cases} 2a^t + k, & if\ x^t = 0; \\ 2a^t - k, & if\ x^t = 1, \end{cases} \quad (6)$$

Obviously, this function can be represented as two subfunctions:

$$f_2^0(a^t) = 2a^t + k; \quad (7)$$

$$f_2^1(a^t) = 2a^t - k. \quad (8)$$

3) The function f_3 corresponds to indirect unconditional jump:

$$f_3(a^t) = a^t - l. \quad (9)$$

In (9), the symbol l stands for some constant value.

Let us point out that these functions correspond only to GSA Γ_1. They can be different in the case of other GSAs.

Let us form a system of equations such that their roots determine the numbers corresponding to state codes. Each equation of the system is equal to the number H of possible transitions. Each transition is determined by one of the functions f_1-f_3.

Of course, any function from the set F can be used for executing some particular transition. But let us use the "transparent" approach. It means that transitions $<a_1, a_2>$, $<a_2, a_3>$ and $<a_6, a_1>$ are executed using the function f_1; the transitions $<a_3, a_4>$ and $<a_4, a_2>$ are executed using the

subfunction f_2^1; the transitions $<a_3, a_5>$ and $<a_4, a_6>$ are executed using the subfunction f_2^0; the transition $<a_5, a_3>$ is executed using the function f_3. Taking it into account, the following system of equations can be created:

$$\begin{cases} a_1 = f_1(a_6); \quad a_2 = f_1(a_1); \\ a_2 = f_2^1(a_4); \quad a_3 = f_1(a_1); \\ a_3 = f_3(a_5); \quad a_4 = f_2^1(a_3); \\ a_5 = f_2^0(a_3); \quad a_6 = f_2^0(a_4). \end{cases} \tag{10}$$

Obviously, the roots of (10) should be integer. The integer values of roots are provided by values k=3, l=7. The solution of the system (10) gives the following state codes: $K(a_1)=10$, $K(a_2)=7$, $K(a_3)=4$, $K(a_4)=5$, $K(a_5)=11$, and $K(a_6)=13$. Now we have a solution for the second step of the method M_1.

The solution of the system (10) can be shown as a graph $G(\Gamma_1)$ (Fig. 4). Its initial, final and operator vertices contain the state codes. The arcs of $G(\Gamma_1)$ are marked by the operations to be executed.

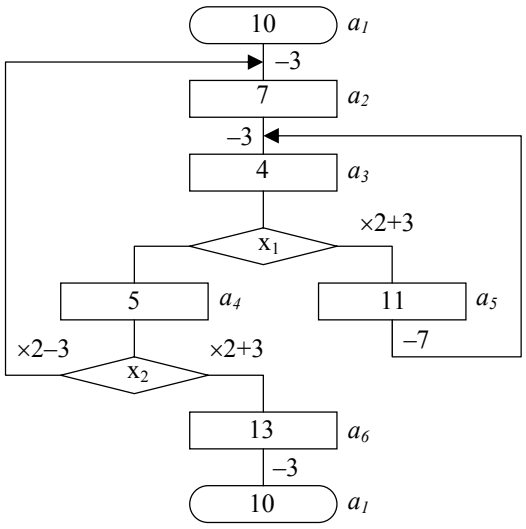

Fig. 4. Graph $G(\Gamma_1)$ corresponding to GSA Γ_1

Let us denote the Moore FSM (Fig. 1) by the symbol U_1, whereas the Moore FSM (Fig. 2) by U_2. Let the symbol $U_i(\Gamma_j)$ mean that the GSA Γ_j is implemented using an FSM U_i ($i = \overline{1,2}$).

There are only M=6 states in the FSM $U_1(\Gamma_1)$, but the maximum value of $K(a_m)$ for $U_2(\Gamma_1)$ if equal 13. Therefore, there is R=3 in the case of $U_1(\Gamma_1)$, but $R=\lceil log_2 13 \rceil=4$ for the FSM $U_2(\Gamma_1)$.

Let us execute the step 3 of the method M_1. Because the outcome of operation f_2 depends on the values of logical conditions, then these conditions should be encoded. Let $K(x_1)=0$ and $K(x_2)=1$, where $K(x_l)$ is a code of a logical condition x_l. It means that the table of BMO for the discussed case should include the one-bit field FX containing the codes of logical conditions. Let us encode the functions $f_S \in F$ using binary codes having R_1 bits where

$$R_1 = \lceil log_2 S \rceil. \tag{11}$$

Let $K(f_1)=00$, $K(f_2)=01$ and $K(f_3)=10$. The table of the block BMO is constructed using the one-hot codes of collections of microoperations $y_n \in Y$, the codes of operations and the codes of logical conditions (Table I).

In this table the codes of states (addresses of cells) are determined by the binary equivalents of the roots of system (10).

The one-hot codes of collections of microoperations (field FY) correspond to the vector $<y_1, y_2, ..., y_5>$, where $y_n \in \{0,1\}$. The symbol * in the table 1 corresponds to the "don't care" situation for a given field. Obviously, there is a redundancy in the block BMO because only 6 from its 16 possible cells are used. The redundancy can be eliminated using the following approach.

TABLE I
CONTENT OF THE BMO OF MOORE FSM $U_2(\Gamma_1)$

a_i	$K(a_i)$	Address	FY	Ψ	Z
		0 0 0 0	*	**	*
		0 0 0 1	*	**	*
		0 0 1 0	*	**	*
		0 0 1 1	*	**	*
a_3	4	0 1 0 0	00100	01	0
a_4	5	0 1 0 1	00110	01	1
		0 1 1 0	*	**	*
a_2	7	0 1 1 1	11000	00	*
		1 0 0 0	*	**	*
		1 0 0 1	*	**	*
a_1	10	1 0 1 0	00000	00	*
a_5	11	1 0 1 1	01100	10	*
		1 1 0 0	*	**	*
a_6	13	1 1 0 1	10011	00	*
		1 1 1 0	*	**	*
		1 1 1 1	*	**	*

Let us delete the second bit from all codes of states $a_m \in A$. It results in obtaining different three-bit codes for states of FSM $U_2(\Gamma_1)$. These codes are the following: $A'(a_1)=110$, $A'(a_2)=011$, $A'(a_3)=000$, $A'(a_4)=001$, $A'(a_5)=111$, and $A'(a_6)=101$. Because all codes are different, they can be used for the unambiguous identification of corresponding cells in the BMO (Table II).

TABLE II
FINAL CONTENT OF THE BMO OF MOORE FSM $U_2(\Gamma_1)$

a_i	$A'(a_i)$	FY	Ψ	Z
a_3	000	00100	01	0
a_4	001	00110	01	1
	010	*	*	*
a_2	011	11000	00	*
	100	*	*	*
a_6	101	10011	00	*
a_1	110	00000	00	*
a_5	111	01100	10	*

The last step of the method M_1 leads to the structure diagram of FSM $U_2(\Gamma_1)$ shown in Fig. 5.

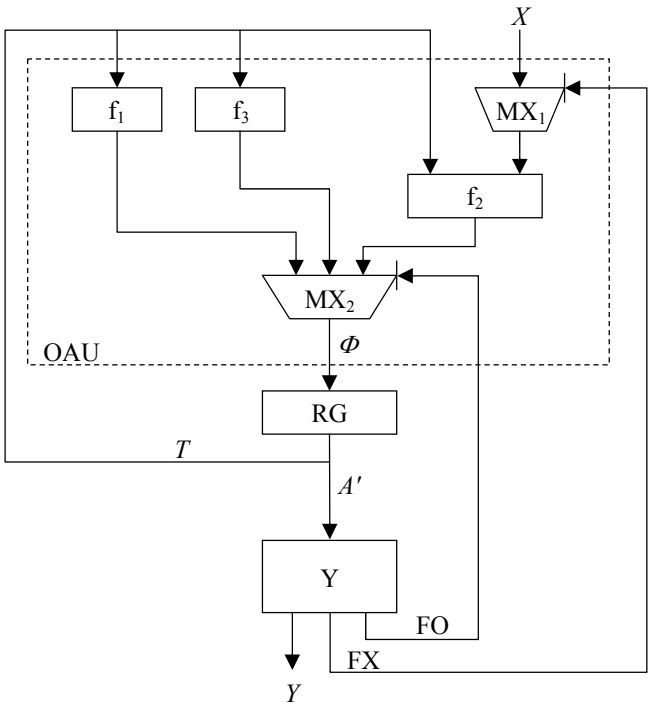

Fig. 5. Structure diagram of FSM $U_2(\Gamma_1)$

Now the minimum possible number of memory blocks (for example, PROMs) is necessary to implement the logic circuit of block BMO. The number of bits can be decreased using well-known methods of encoding of the collections of microoperations [13]. But these methods are beyond the scope of this article.

In FSM $U_2(\Gamma_1)$, the operational blocks f_1-f_3 implement the corresponding functions (5), (6), and (9). It is necessary to use a shifter one position to the left to multiply a state code by 2 [12]. If the numbers k, l are represented in the two's-complement form, then all other operations can be executed using a binary adder [12]. The multiplexor of logical conditions MX_1 generates the values of a logical condition $x_l \in X$ to be checked. The code $K(x_l)$ is represented by the field FX. The multiplexor MX_2 chooses one from three possible codes of the next state. The choice is determined by the code from the field FO. The first, third and fourth bits of $K(a_m)$ form the address A' used for choosing a particular cell of BMO.

In the discussed example, we use the simplest possible structure of OAU. We merely wanted to illustrate the main principles of organization and design for proposed FSM with operational addressing. We do not discuss the method M_2 in this article because it is very similar to the method M_1.

V. Investigation of Moore FSM with Operational Addressing

Let us use the minimum hardware amount as an efficiency criterion of a particular FSM model. Let us compare the hardware amount for blocks BIMF and OAU for equivalent FSMs. Let us use two-input gates as equivalent gates (EG) to make the required comparison.

Let the block BIMF of Moore FSM U_1 implement the system of Boolean functions (1). Let these functions be represented in the sum-of-product (SOP) form [2]. The number of equations in (1) is equal to R, where the value of R is determined by (2). Let R_{LC} be an average number of logical conditions in each term of the system (1). It means each term is represented by a conjunction having $R_T=R_{LC}+R$ literals. Obviously, it is necessary H_1 equivalent gates to implement each term:

$$H_1 = R_T - 1 = R_{LC} + R - 1. \quad (12)$$

Let each equation $D_t \in \Phi$ includes T terms. This value corresponds to the amount of different paths in a GSA Γ (different interstate transitions). Then, the number of EGs necessary to combine T terms is equal to

$$H_2 = T - 1. \quad (13)$$

The system Φ includes R functions; therefore, the value RH_1 corresponds to a hardware amount necessary for implementing one transition. The value RH_2 determines the hardware amount necessary for implementing the interterm connections for all equations of (1). Taking into account that a GSA includes T transitions, the total amount of EGs in the logic circuit of BIMF is determined as

$$H_K = R(TH_1 + H_2) = R(T(R_{LC} + R - 1) + T - 1). \quad (14)$$

Usage some optimization methods [2] leads to decreasing the value of H_K. To take it into account, let us introduce a coefficient of minimization $k_1=(0,1]$. Now the formula (14) is transformed into the following one:

$$H_K = k_1 R(T(R_{LC} + R - 1) + T - 1). \quad (15)$$

Let us estimate the hardware amount in the logic circuit of Moore FSM U_2. Let us represent the hardware amount for OAU as

$$H_{OAU} = H_3 + H_4. \quad (16)$$

In (16), the symbol H_3 stands for the hardware amount required by operational blocks f_1-f_S and the symbol H_4 for implementing the multiplexor MX_2.

The value of H_3 depends on both the number of different operations of transitions and their complexity. To rough estimation of hardware amount in OAU, let us consider an average hardware amount H_{OP} for implementing one operation of transition. In this case, the value of H_3 is determined as

$$H_3 = S \cdot H_{OP}. \quad (17)$$

Let us point out that each new transition increases H_K by some value H_T, where

$$H_T = R \cdot H_1. \quad (18)$$

The value of (18) is constant for constant values of R and R_{LC}. In the case of OAU, the situation is a bit different. If this new transition cannot be implemented using already existed operational blocks (OB), then some new OB should be introduced. It increases H_{OAU} by the value H_{OP}. This value is a constant too (if the growth of hardware in MX_2 is neglected).

Let us introduce some coefficient k_2 in (17). It is used for representing H_{OP} through H_T:

$$H_{OP} = k_2 H_T = k_2 R H_1. \quad (19)$$

The value S in (17) is the most difficult for forecasting. It depends on many factors such as the structure of GSA and types of OBs to be used. Of course, the value of S is some function on T (the number of transitions), but it is impossible to find the exact universal function $S(T)$ correct for any GSA Γ. It is connected with the heuristic approach used for choosing both types and numbers of operations of transitions in the case of each GSA Γ.

We conduct some experimental investigations allowing making the following conclusions. If $T \in [0, 10]$, then a new operation is added for approximately 2 new transitions. It means that $S \approx T/2$. If $T \in [10, 30]$, then a new operation is added for 5-7 new transitions. If $T \in [30, 100]$, then it is added for 10-20 transitions and so on. This dependence can be represented as the following expression:

$$S = k_3 \ln(T/2) + 2. \quad (20)$$

In (20), the coefficient k_3 was obtained in the experimental way. For different GSAs, it belongs to interval from 2,5 to 5.

Using (19) and (20), the expression (17) can be represented as

$$H_3 = (k_3 \ln(T/2) + 2) k_2 R H_1). \quad (21)$$

The multiplexor MX_2 generates the code of the next state (R bits) and it is controlled by the code from FO having $R_S = \lceil \log_2 S \rceil$ bits. Each output of MX_2 generates a SOP having S terms. Taking into account the interterm disjunctions, the number of EGs required for implementing the MX_2 is determined as:

$$H_4 = R(S \cdot \lceil \log_2 S \rceil + S\text{-}1. \quad (22)$$

Using (21) and (22), the following expression can be obtained for (16):

$$H_{OAU} = (k_3 \ln(T/2) + 2) k_2 R H_1 + R(S \lceil \log_2 S \rceil + S\text{-}1). \quad (23)$$

Let us find the efficiency of OAU respectively to BIMF of equivalent Moore FSM U_1 as the following relation:

$$E_{OAU} = H_K / H_{OAU}. \quad (24)$$

Obviously, if $E_{OAU} > 1$, then OAU has less amount of hardware than BIMF.

Let us find the dependence of E_{OAU} from different parameters affecting the circuits of both OAU and BIMF. Let us use the following values for constants: $R=10$, $T=2000$, $R_{LC}=2$, $k_1=0,8$, $k_2=30$, and $k_3=3,5$.

The function $E_{OAU}(T)$ is shown in both Table III and Fig. 6.

TABLE III
TABULAR FORM OF FUNCTION $E_{OAU}(T)$

T	E_{OAU}	T	E_{OAU}
200	0,32	1200	1,41
400	0,56	1400	1,60
600	0,78	1600	1,80
800	1,00	1800	2,00
1000	1,20	2000	2,18

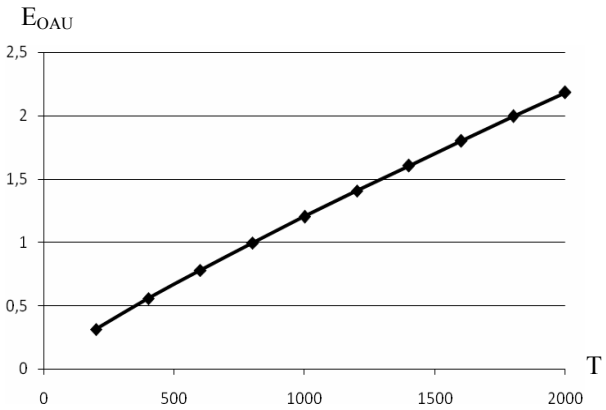

Fig. 6. Dependence of E_{OAU} from the number of transitions T

As follows from both Table III and Fig. 6, this function is linear. The FSM U_2 becomes more effective when $T>800$. The further growth of the number of transitions leads to growth of the gain.

The function $E_{OAU}(R)$ is shown in both Table IV and Fig. 7.

TABLE IV
TABULAR FORM OF FUNCTION $E_{OAU}(R)$

R	E_{OAU}	R	E_{OAU}
3	2,43	10	2,18
4	2,35	15	2,14
5	2,30	20	2,11
6	2,26	25	2,10
7	2,24	30	2,09

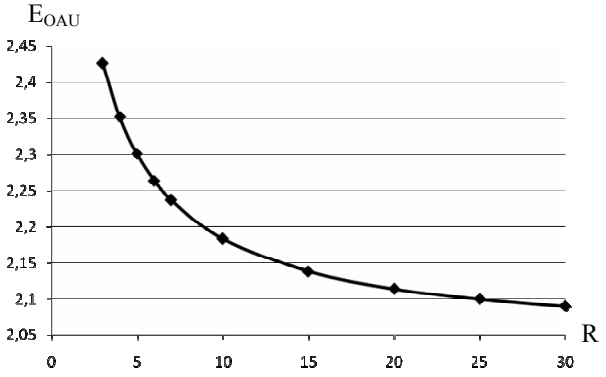

Fig. 7. Dependence of E_{OAU} from the number of transitions R

Analysis of both Table IV and Fig. 7 shows that this function is restricted by the value 2,05. So, the circuit of OAU always needs less amount of equivalent gates than the circuits of BIMF.

The function $E_{OAU}(k_1)$ is shown in both Table V and Fig. 8.

TABLE V
TABULAR FORM OF FUNCTION $E_{OAU}(K_1)$

k_1	E_{OAU}	k_1	E_{OAU}
0,3	0,82	0,6	1,64
0,35	0,96	0,7	1,91
0,4	1,09	0,8	2,18
0,45	1,23	0,9	2,46
0,5	1,36	1,0	2,73

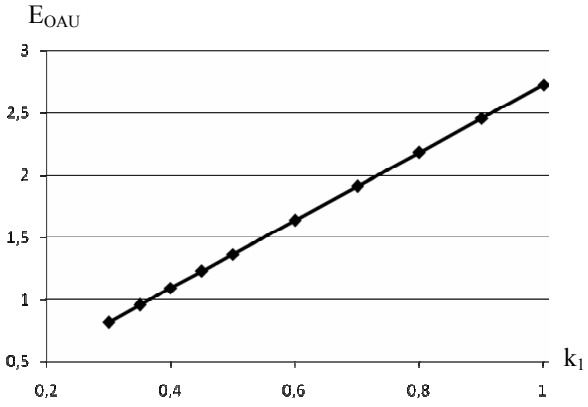

Fig. 8. Dependence of E_{OAU} from the coefficient k_1

As follows from both Table V and Fig. 8, the increasing of coefficient of minimization for functions Φ leads to the linear growth of the efficiency E_{OAU}. If $k_1=1$ (no minimization is possible), then E_{OAU} reaches its maximum value equal to 2,73. Only in the cases when the usage of minimization simplifies the system Φ up to 60% the application of FSM U_1 makes sense.

The function $E_{OAU}(k_2)$ is shown in both Table VI and Fig. 9.

TABLE VI
TABULAR FORM OF FUNCTION $E_{OAU}(K_2)$

k_2	E_{OAU}	k_2	E_{OAU}
10	6,32	60	1,10
20	3,25	70	0,95
30	2,18	80	0,83
40	1,64	90	0,74
50	1,32	100	0,66

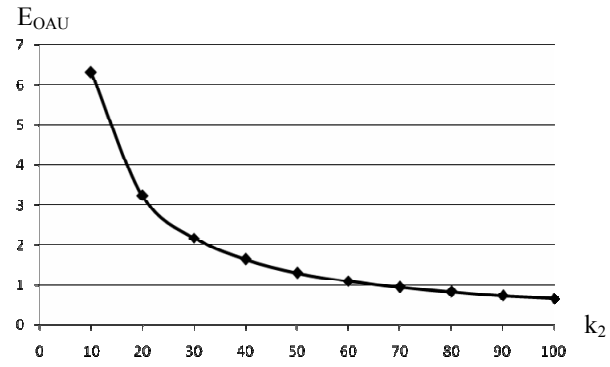

Fig. 9. Dependence of E_{OAU} from the coefficient k_2

As follows from both Table 6 and Fig. 9, the growth of the average complexity of operational blocks used for executing transitions leads to decreasing of the efficiency of FSM U_2. For used values of arguments, out approach can be applied till $k_2<65$.

At last, the function $E_{OAU}(k_3)$ is shown in both Table VII and Fig. 10.

TABLE VII
TABULAR FORM OF FUNCTION $E_{OAU}(K_3)$

k_3	E_{OAU}	k_3	E_{OAU}
1	6,44	6	1,31
2	3,62	7	1,13
3	2,51	8	0,99
4	1,93	9	0,89
5	1,56	10	0,80

The nature of this diagram is determined by the influence of k_3 on the value of logarithmic function (20). The growth of k_3 leads to increase for the number of operational blocks. If $k_3<8$, then the proposed approach makes sense. Let us point out that an appropriate choice of operations of transitions leads to decrease of k_3.

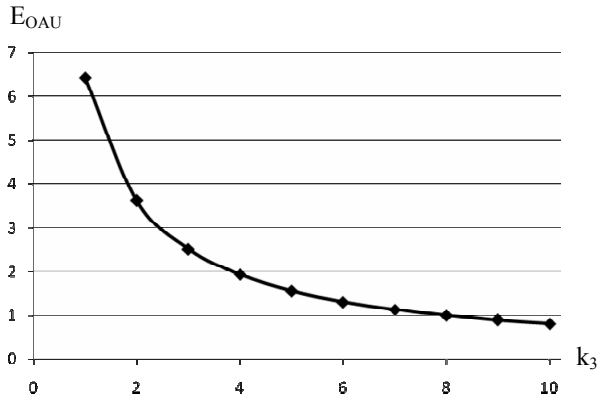

Fig. 10. Dependence of E_{OAU} from the coefficient k_3

Analysis of functions shown in Fig. 6 – Fig. 10 allows making the following conclusions. The following factors provide increasing for the efficiency of FSM with operational addressing in comparison with known models of Moore FSM:

1. The growth of the amount of transitions: the FSM with OA should be applied for implementing complex control algorithms.
2. The decrease of the value of bits in the states codes: in the ideal case these values should be equal for both equivalent Moore FSM and FSM with OA.
3. Implementing control algorithms with small rate of minimization.
4. The decrease for the average complexity of operational blocks used for implementing the operations of transitions.

VI. CONCLUSION

Application of the proposed approach of operational addressing allows implementing logic circuits of control units using only standard library elements of CAD libraries. This

approach targets mostly FPGA- and ASIC-implementations of control units. This approach can decrease the hardware amount and increase performance of resulting control unit in comparison with known design methods. Of course, it is possible if some conditions discussed in our article take place.

Our investigations show that this approach should be applied for rather complex finite state machines having more than 80-100 states. But the growth of gain (hardware reduction) is possible only if each operational block executes more than one transition. It requires developing new state assignment algorithms targeting the proposed organization of control units.

Now, the authors develop design methods targeting usage more than one logical condition for executing the interstate transitions of Moore FSM. It permits the one-cycle execution of multidirectional transitions by the Moore FSM with operational addressing. Also, we develop methods for finding the set of operations leading to further saving the number of LUT elements in the logic circuits of Moore FSMs with operational addressing.

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A Flexible Design for Optimization of Hardware Architecture in Distributed Arithmetic based FIR Filters

Fazel Sharifi, Saba Amanollahi, Mohammad Amin Taherkhani and Omid Hashemipour

Abstract — **FIR filters are used in many performance/power critical applications such as mobile communication devices, analogue to digital converters and digital signal processing applications. Design of appropriate FIR filters usually causes the order of filter to be increased. Synthesis and tape-out of high-order FIR filters with reasonable delay, area and power has become an important challenge for hardware designers. In many cases the complexity of high-order filters causes the constraints of the total design could not be satisfied. In this paper efficient hardware architecture is proposed for distributed arithmetic (DA) based FIR filters. The architecture is based on optimized combination of Look-up Tables (LUTs) and compressors. The optimized system level solution is obtained from a set of dynamic-programming optimization algorithms. The experiments show the proposed design reduced the delay cost between 16%-62.5% in comparison of previous optimized structures for DA-based architectures.**

I. Introduction

Nowadays, FIR filters, regarding to their superior properties such as stability and high reliability in digital signal processing, have had many important and widespread applications. This kind of digital filters are applied to an extensive form in many areas such as image processing, radio communication and high technology devices. One of the important applications of FIR filters is in analog to digital converters [1][2]. Also FIR filters are applied in read channel of disc drives known as PRML [3] in addition to wideband receivers in wireless communication devices [4].

Generally in an *N*-order FIR filter with $coef[i]\ \forall i \in [0, N-1]$, the output *y[t]* is calculated according to the current input *x[t]* and previous inputs $x[t-i]\ \forall i \in [1, N-1]$ by equation (1):

$$\begin{aligned} y[t] &= \sum_{i=0}^{N-1} coef[i]x[t-i] \\ &= coef[0]x[t] + coef[1]x[t-1] + \ldots + coef[N-1]x[t-N+1] \end{aligned} \quad (1)$$

As it is shown in equation (1), in each step for calculation of *y[t]* as the output of *N*-order filter, *N* additions and *N* multiplications are required.

Although the FIR filters are more stable compared to IIR filters, their circuits are very complicated due to necessity of designing high order FIR filters in real application. By increasing in order of filter, the circuit is become more complicated and this is one of the most important challenges in front of designing these types of filters. This complexity sometimes causes desired design does not meet area, timing and power constraints.

In this paper a compound architecture for FIR filters is proposed. Considered modules in the proposed architecture are optimized by efficient algorithms and final architecture will be extracted.

The rest of this paper includes following sections. In section 2, architectures of FIR filter with related works are reviewed. In section 3 the proposed architecture is introduced. Optimization algorithms for construction of efficient hardware architecture are introduced in section 4. Experimental results are shown in 5 and finally section 6 concludes the paper and future works are considered.

II. A review of related architectures

For implementation of FIR filter structures, hardware architectures based on multiply and add (MAC) and distributed arithmetic (DA) are known as the main classes of FIR filter architectures.

In MAC-based architectures, computation of the desired output is done directly and it is based on multiplication and addition. To improve the performance of MAC-based architectures, some researches focused on design of filters based on Residue Number system (RNS)

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[5]-[7]. In these designs, processing overhead and hardware cost of binary to RNS conversion should be considered.

Complexity of classic multiplication and addition causes a lot of researches tend to change in filter architecture and be done based on DA, so that without using multipliers, the idea of pre-computing and storing the required values has been exploited.

The classic method of distributed computing works based on changing the form of required computations in equation (1) and rewriting it in new computation forms. For this purpose it assumes, the states $x[k]\ \forall k \in [t-N+1, t]$ in binary standard format (2`s complement) and has been scaled ($|x[k]| < 1$) and it can be shown by the following equation:

$$x[k] = -x_{B-1}[k] + \sum_{j=0}^{B-2} x_j[k] 2^{-j} \qquad (2)$$

Substituting equation (2) in equation (1) results to:

$$y[t] = \sum_{i=0}^{N-1} coef[i](-x_{B-1}[t-i]) + \sum_{j=0}^{B-1} 2^j \times (\sum_{i=0}^{N-1} coef[i].x_j[t-i]) \qquad (3)$$

A look up table could be used with N-bit input address to preserve the value of $\sum_{i=0}^{N-1} \text{coef[i]}.x_j[t-i]$. In This condition, size of LUT size (without applying optimization) would be $2^N \times (C + \log_2^N)$, where N is the order of filter C is the length of coefficients in binary form. As the equation 3 shows, a combination of sum of coefficients can be calculated in advance and be stored in look up tables.

The main problem of look-up tables is the complexity of table size which grows exponentially by increasing of filter order. A method have been proposed in [9] to reduce (and ultimately eliminate) the size of required look-up table. But in the proposed LUT-less architecture, the delay of adders and multiplexers (MUX) is not considered and therefore the solution is not efficient for performance-critical applications. In [10] another DA-based FIR filter has been presented that is suitable for FPGA platforms with 4-input look-up tables.

III. Proposed Architecture

As it has been shown in previous section, distributed arithmetic based architectures face off with exponential complexity problem for the size of look up tables. In this section an efficient architecture is presented in order to increase performance of computation part of digital filters. As it is illustrated in Figure 1, main components of proposed architecture are formed based on a compound model with two main layers including look up tables and compressors. As it can be seen in Figure 1, N bits are used in first layer of shift register and $k = \sum_{i=1}^{m} k_i$ bits out of these N bits are assigned to M look up tables, with $k_1 \ldots k_m$ inputs. In the next section, an optimization algorithm for finding efficient structure for look up tables set with k bits input address is introduced.

Remaining bits (N-k) are used as selectors in 2-1 multiplexers (for every bit) and totally $C \times (N-k)$ multiplexers are required. If the selector of i^{th} multiplexer becomes 1 the related coefficient will be added to compressor part.

M outputs of look up tables with N-k outputs of multiplexers are used as inputs of N-k+m:2 compressor. The functionality of the compressor is shown in Figure 2. Extraction of an efficient N-k+m:2 compressor is described in the next section. After compression, a CLA adder is used for final summation.

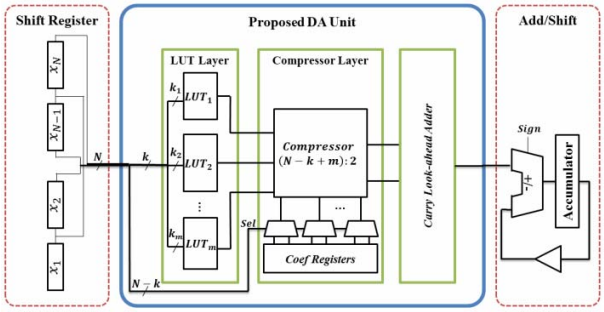

Fig. 1. Proposed Architecture for Distributed Arithmetic Unit

It should be considered that look up table's layers and compressors can be used alone without each other. In the other hand optimized architecture can work without compressor (Partitioned-LUT) or without look up tables (LUT-less). In the next section, three algorithms have been proposed to identify the optimum architecture.

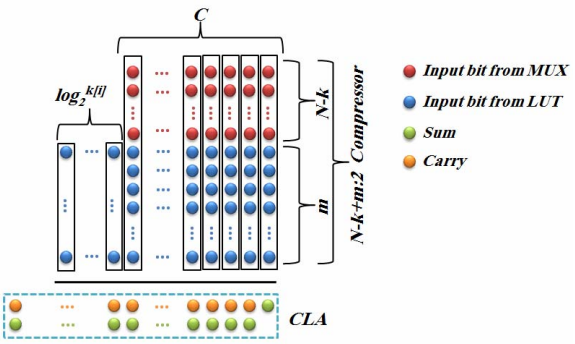

Fig. 2. Functionality of the designed Compressor Layer

IV. Architecture Extraction Algorithms

As was noted in the previous section, the proposed approach provides possibility of choosing suitable hardware architecture based on compound structure sets

in a flexible way. For finding efficient architecture the following parameters should be determined precisely:

- Optimized structure of LUT set based on input parameter (k): In this section k_i and m values are chosen somehow LUT size with k bit input address is optimized. The proposed algorithm is presented in section 4.1.
- Optimized compressor structure based on input bits set (h): In this section optimized compressor structure is extracted based on small-optimized compressors. The proposed algorithm is presented in section 4.2.
- Final optimized architecture: In this section, according to parameter values for LUTs and compressors, number of input addresses for the LUT layer and number of selector bits for compressor layer are chosen in a way which the final architecture is optimized. Final optimization algorithm is proposed in section 4.3.

Optimization could be done based on following parameters:

- Gate latency: in all optimizations process delay of XOR gate is considered as the delay unit. This parameter is shown by (2ΔG).
- Power consumption: optimization for power consumption is based on minimum number of resources and could be determined by power consumption unit of XOR gate.
- Power-delay product (PDP): the proposed algorithms could be extended to optimize PDP parameter based on previous parameters.

4.1. Optimization of LUT Layer

In this section, technique has been proposed for partitioning of LUTs. In this work the LUT layer with k bits for input addresses and m outputs is partitioned into m basic LUTs based on computation of delay/power and power delay product (PDP) parameters in gate level. LUT models based on Decoder-Memory are exploited for description of architecture in the LUT layer [14].

The structure of a basic LUT with k_i input address (for preserving the summation of k_i coefficients) contains a k_i to 2^{ki} decoder and a 2^{ki} words memory with $C + [\log_2^{k_i}]$ length. Suppose, delay of this LUT is notated as $d_{lut\ k[i]}$, and its power consumption and power delay product (PDP) are respectively notated as $p_{lut\ k[i]}$ *and* $pdp_{lut\ k[i]}$.Therefore for a LUT layer with the k inputs and m outputs, the structure with optimized delay ($D(LUT_{k,m})$) or optimized power ($P(LUT_{k,m})$) or optimized PDP ($PD(LUT_{k,m})$) could be obtained from the dynamic programming Algorithm 1 with $O(n^2)$ complexity.

4.2. Optimization of Compressor Layer

In this section a method is proposed for auto construction of the *h:2* optimized compressor based on delay, power and PDP parameters. Creating large input compressors are carried out by using of optimized conventional and unconventional compressors [11]-[13].

Therefore, for creating an optimized large input compressor (*h:2*), set of F basic compressors $Comp_i \ldots Comp_F$ with compression levels $(I_{Comp[k]} : O_{Comp[k]})\ \forall k \in [1..F]$ are used. Unconventional compressors have some carry in and carry out bits. However, these carry bits are created in such a way in compressor which there are not carry propagation. Suppose delay, power and PDP of basic compressor k are $d_{Comp[k]}$, $p_{Comp[k]}$, $pdp_{Comp[k]}$ respectively.

OptimizeLUT (Address Bits: k, Number of LUTs :m):
1. D(LUTi,1)←dlut[i]; $\forall i \in [1..k]$
2. P(LUTi,1)← plut[i]; $\forall i \in [1..k]$
3. PD(LUTi,1)← pdlut[i]; $\forall i \in [1..k]$
4. for (i=2; i <= k; i++)
5. for (j=2; j <= m; j++)
6. D(LUTi,j)←minu{max{dlut[u] , D(LUTi-u,j-1)}};
7. P(LUTi,j)←minw{plut[w]+P(LUTi-w,j-1)};
8.PD(LUTi,j)←min{D(LUTi,j).Pu(LUTi,j),Dw(LUTi,j).P(LUTi,j)};
end for
end for
return D(LUTk,m), P(LUTk,m), PD(LUTk,m);

Algorithm 1. Proposed Algorithm for Optimization of LUT layer

The problem of finding minimum Delay ($D_{h,2}(k)$-which describes minimum delay of h:2 compressor with basic compressors $Comp_1 \ldots Comp_k$) or minimum Power ($P_{h,2}(k)$) or minimum PDP ($PDP_{h,2}(k)$) could be followed by two different configurations. In one configuration, the $Comp_k$ is not used and therefore the best solution may be gathered from previous calculations $D_{h,2}(k\text{-}1)$, $P_{h,2}(k\text{-}1)$, $PDP_{h,2}(k\text{-}1)$. But the other way is usage of $Comp_i$. In this condition, the compressor is divided into 3 sub-modules as shown in Figure 3. These modules are the basic compressor $Comp_k$ and two compound compressors $h\text{-}I_{Comp[k]}$*:g and* $O_{Comp[k]}$+*g:2*. The optimum solution is obtained from minimum of these two configurations. The proposed dynamic programming approach with polynomial complexity is shown in Algorithm 2.

4.3. Extraction of final solution

In this step, based on optimization results of the LUT layer and the compressor layer, the final architecture of the proposed DA unit is extracted. In other word the value for m and k is determined by using the Algorithm 3.

Based on the main criteria for the designer, the algorithm could present separately the optimized solution for delay, power or PDP parameters. As shown in

Algorithm 3, the cost function could be any arbitrary parameters Delay, Power or PDP returned from *OptimizedLUT* and *OptimizedComp* Algorithms.

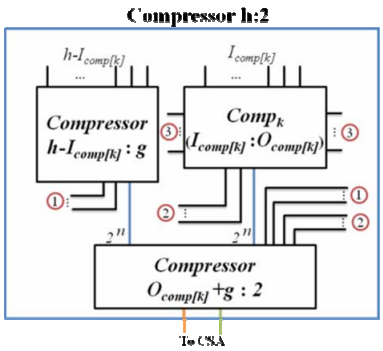

Fig. 3. A configuration of h:2 compressor exploiting the basic compressor $Comp_k$

```
OptimizeComp (CompLevel: h):
F← Number of basic Compressors
Di,j(0)←∞;  Pi,j(0)←∞;  PDPi,j(0)←∞;  ∀i ∈ [1..h], j < i
Di,j(k)←0;  Pi,j(k)←0;  PDPi,j(k)←0;
∀k ∈ [1..f], i ∈ {1,2}, j < i
while (k < F)
  for (i=3; i <= h; i++)
    for (j=1; j  < i; j++)
      if((i:j) = (I Comp[k]: O Comp[k]))
        Di,j(k) ← dComp[k];
        Pi,j(k) ← pComp[k];
     PDPi,j(k)← pdpComp[k]
    else
     Dmin←minu{max{Di-I  Comp[k],u(k),  dComp[k]}+DO
Comp[k]+u.2(k)};
      Pmin←minw{Pi-I  Comp[k],u(k)  +  POComp[k]+u.2(k)+
pComp[k] };
     TP←ComputePower(u); TD←ComputeDelay(w);
     Di,j(k) ← min{Di,j(k-1), Dmin};
     Pi,j(k) ← min{Pi,j(k-1), Pmin};
    PDPi,j(k) ← min{Di,j(k-1). Pi,j(k-1), Dmin.TP, Pmin.TD};
   end for
 end for
```

Algorithm 2. Optimization of Compressor Layer

```
OptimizeArch (Filter Order: N):
OptSolution←∞;
Select cost from {Delay | Power | PDP}
for (i=1; i <= N; i++)
  for (j=1; j <=i; j++)
    ArchCost  =  cost(OptimizeLUT(i,j),  OptimizeComp(N-
i+j));
    if  (ArchCost<OptSolution)
      OptSolution←ArchCost;
   end for
end for
```

Algorithm 3.Extraction of optimized architecture

V. Implementation and Experiments

Implementation has performed in two sections. In first section, hardware description of all basic components has been implemented. Verilog implementation of basic optimized compressors includes 3:2, 4:2, 5:2, 6:2, 7:2 and 9:2 compressors [11]-[13]. The other regular compressors such as 7:3 or 15:4 could be constructed from these basic components. The implementation of basic LUTs was based on memory model in CACTI 5.1 [14]. In the second section of this phase, the optimized architecture algorithms have been implemented in 9 source and header files to present the optimized structure of DA unit.

The real coefficients have been extracted from Filter Design and Analysis Tool (FDATool) [15]. The coefficients are produced for implementation of the sample filters listed in Table 1. As shown in the table based on the supplied criteria, the order of filter is determined from 8 to 143. According to our requirements in application of designing digital part of ADCs, the frequency of sampling (F_s) and length of inputs (B) have been set to a 40MHz and 3 bits respectively. In addition, in all design C (length of coefficients) is set to 16 bits.

Table I
Specification of Analyzed FIR Filters

Filter Order	F_S (MHz)	F_{Pass}/ F_{Stop} (MHz)	A_{Pass}/ A_{Stop} (dB)
8	40	1.2/3.8	3/20
18	40	1.2/3.8	3/40
31	40	1.6/3.0	3/40
72	40	2.2/2.8	3/40
108	40	2.2/2.8	3/60
143	40	2.2/2.8	3/80

The estimated delay based on (Gate delay-ΔG) for Distributed Arithmetic unit of LUT, LUT-less [9] and proposed architectures is shown in Figure 4. LUT-less architecture in [9] is implemented by full compressors instead of regular adders. As shown in the figure delay of the proposed architecture is 16% (for 8-order filter) to 62.5% (for 143-order filter) less delay in comparison of LUT-less architecture.

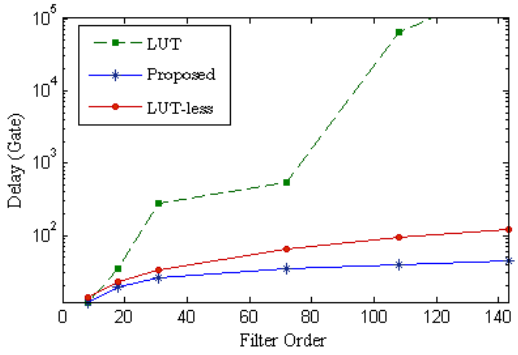

Fig. 4. Estimated Delay of FIR filters for DA-based architectures

VI. Conclusion and Future Works

According to design constraints in high-order FIR filters, in this work the following contributions were presented:

- Compound hardware architecture was proposed for distributed arithmetic based FIR filters. The architecture exploits the benefits of pre-served summation in optimized LUTs and improves the speed of addition by using high efficient compressors.
- A dynamic programming algorithm was proposed with polynomial complexity to find the optimized structure of compressors.
- A dynamic programming algorithm was proposed to find the best solution for LUT partitioning.
- The final optimized architecture could be extracted from third-proposed algorithm.

For the future works, we will attempt to extend the tool which is capable for automatic generation of HDL code for the optimized extracted architecture.

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Application of Multi-Scale PCA and Energy Spectrum to Bearing Fault Analysis and Detection in Rotating Machinery

K. Baiche, M. Zelmat, A. Lachouri

Abstract – **This paper introduces various works on fault detection of rotating machines caused by bearings damage. The novelty of this work is the application of new scheme based on the multi-scale principal component analysis MSPCA, and the energy spectrum of details coefficients of the discrete wavelet transform (DWT). The DWT coefficient details are calculate in first stage in order to be used as inputs of the MSPCA scheme and in the second stage they are used to evaluate the spectrum energy.**

Keywords: **Fault analysis, rotating machinery, MSPCA, wavelet transform, spectrum energy, bearing diagnosis.**

I. Introduction

Rolling element bearings are essential elements in most rotating machines. Bearing failures are prone to cause both personal damage and economic loss if not be detected well in advance [1-5]. To avoid such catastrophic failures, it is necessary to develop and implement efficient diagnosis monitoring systems that are independent of operating conditions. Therefore, a significant amount of research efforts have focused on the predictive maintenance of machines. Machine Vibration Signature Analysis (MVSA) provides an important way to assess the health of a machine.

In traditional MVSA, the Fourier transform is used to determine the vibration spectrum. Typically, frequencies of bearing defects are identified and compared with initial measurements to detect any deterioration in bearing health.

In recent years [5], different technologies have been used in order to process signals produced by dynamical systems. Most of the authors classify the analysis of vibration signature in three approaches. The first one is the time domain, based on statistical parameters such as mean, root mean-square, variance, kurtosis, etc. The second approach proceeds in the frequency domain, where the Fourier transform and its numerous variants have been intensively used. The shortcoming of this approach is that Fourier analysis is theoretically limited to stationary signals, whilst bearing vibrations are typically non-stationary by nature [6]. The third approach is based on the time-frequency analysis such as the short-time Fourier transform (STFT) or the (discrete) wavelet transform (DWT). It has been successfully applied as a fault feature extractor due to its good energy concentration properties. Besides, in the diagnosis field, methods based on the information redundancy concept have been developed. Generally, these methods rest on a consistency test between an observed behavior of the process provided by sensors and a mathematical representation. The comparison between these behaviors produces residual quantities that serve to discriminate normal plant operation from an abnormal situation.

In this work, experimental vibration signals for both normal and faulty bearings are acquired. Then a feature vector is generated to be applied as the inputs to a MSPCA according the processing flowchart in Fig.1. The square prediction error (SPE) calculated from the MSPCA method and the spectrum Energy (SE) indicate the difference between the healthy and the defective bearing.

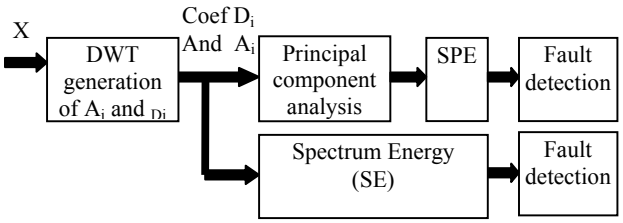

Fig. 1. Processing flowchart

This manuscript develops two methods based on the spectrum energy and the MSCPA. Principal components analysis (PCA) is a projection based on statistical methods used for dimensionality reduction. It is a descriptive technique which permits the study of the relations existing between variables without taking account of any a priori structure [7].

The discrete wavelet transform (DWT) provides an efficient method for generating feature vectors. The DWT coefficients can be used to generate statistical parameters from each resolution level of the transform. These coefficients capture trends within the sensors at the corresponding scale [8]. They serve as efficient inputs to be fed to a decision system, such a Neural Network.

The remainder of this paper is organized as follows. The next section describes the characteristic vibration frequencies of bearings. Section III presents the experiment setup and section IV describes the PCA, wavelets and MSPCA methods. The Section V describes the spectrum Energy and the Section VI presents the simulation, and experimental results, respectively. The conclusion is given in section VII.

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II. Characteristic vibration frequencies

The characteristic vibration frequencies due to bearing defects can be calculated from the rotor speed and bearing geometry. The typical rolling element bearing geometry is displayed in Fig.2. Characteristic vibration frequency $f_V$can be calculated using (1)-(4) [1], [2].

The outer race defect frequency, f_{OD} -the ball passing frequency on the outer race- is given by,

$$f_{OD} = \frac{n}{2} f_{rm}\left(1 - \frac{BD}{PD}\cos\varphi\right) \quad (1)$$

where φ is the contact angle, PD is the pitch diameter, BD is the ball diameter, n is the number of balls, and f_{rm} is the rotational speed.

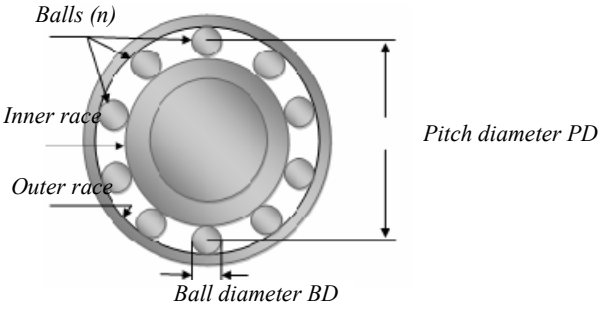

Fig. 2. Rolling element bearing geometry

The inner race defect frequency, f_{ID}-the ball passing frequency on the inner race- is given by,

$$f_{ID} = \frac{n}{2} f_{rm}\left(1 + \frac{BD}{PD}\cos\varphi\right). \quad (2)$$

The ball defect frequency, f_{BD} - the ball spin frequency - is given by

$$f_{BD} = \frac{PD}{2BD} f_{rm}\left(1 - \left(\frac{BD}{PD}\right)^2 \cos^2\varphi\right). \quad (3)$$

The train defect frequency, f_{TD}-caused by an irregularity in the train- is given by,

$$f_{TD} = \frac{1}{2} f_{rm}\left(1 - \frac{BD}{PD}\cos\varphi\right). \quad (4)$$

The characteristic current frequencies, f_{CF}-due to the bearing characteristic vibration frequencies, f_v- are calculated by

$$f_{CF} = \left|f_e \pm m f_v\right| \quad (5)$$

where m=1, 2, 3, and $f_e$is the power line frequency. This latter equation represents an amplitude modulation of the stator current by the bearing vibrations. Equations (1)-(5) can be used to calculate the current spectral components due to faulty bearings.

III. Description of the experiment

As shown in Fig.3, the test stand consists of a 2 HP motor (left), a torque transducer/encoder (center), a dynamometer (right), and control electronics (not shown). The test bearings support the motor shaft. Single point faults were introduced to the test bearings using electro-discharge machining with fault diameters of 7 mils (1 mil=0.001 inches) and depth of 110 mils in inner race. SKF bearings were used. Drive end (6205-2RS JEM SKF, deep groove ball bearing) and fan end (6203-2RS JEM SKF, deep groove ball bearing) bearing specifications, including bearing geometry and defect frequencies are listed in Tables I-IV. Vibration data was collected using accelerometers, which were attached to the housing with magnetic bases.

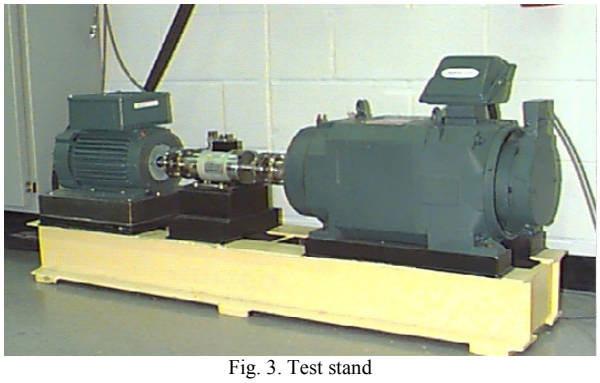

Fig. 3. Test stand

Table I
Drive end bearing geometry (size in inches)

Inside Diameter	Outside Diameter	Thickness	Ball Diameter	Pitch Diameter
0.9843	2.0472	0.5906	0.3126	1.537

Table II
Defect frequencies (multiple of running speed in Hz) for Drive end bearing

Inner Ring	Outer Ring	Cage Train	Rolling Element
5.4152	3.5848	0.39828	4.7135

Table III
Fan end bearing geometry (size in inches)

Inside Diameter	Outside Diameter	Thickness	Ball Diameter	Pitch Diameter
0.6693	1.5748	0.4724	0.2656	1.122

Table IV
Defect frequencies (multiple of running speed in Hz) for Fan end bearing

Inner Ring	Outer Ring	Cage Train	Rolling Element
4.9469	3.0530	0.3817	3.9874

Accelerometers were placed at the 12 o'clock position at both the drive end and fan end of the motor housing. During some experiments, an accelerometer was attached to the motor supporting base plate as well. Vibration signals were collected using a 16 channel DAT recorder. Digital data was collected at 12,000 samples per second, and data was also collected at 48,000 samples per second for drive end bearing faults. Speed and horsepower data were

collected using the torque transducer/encoder and were recorded by hand. Outer raceway faults are stationary faults; therefore placement of the fault relative to the load zone of the bearing has a direct impact on the vibration response of the motor/bearing system. In order to quantify this effect, experiments were conducted for both fan and drive end bearings with outer raceway faults located at 3 o'clock (directly in the load zone), at 6 o'clock (orthogonal to the load zone), and at 12 o'clock. The rotation speed (frequency) of the shaft is approximately 1750 rpm (29,2 Hz).

IV. PRINCIPAL COMPONENT ANALYSIS AND WAVELETS

Generally, the fault detection based on analytic model corresponds to the generation of a residual between normal plant operation and available measurements. From the residual analysis, we can make a decision to indicate whether the failure is present or not.

In this section, the general principles of using PCA for fault detection are presented. It is followed by a brief introduction to wavelets. This section prepares the basic concept of the MSPCA which is explained in the next section.

4.1 Principal component analysis

Principal component analysis (PCA) has been introduced by Pearson and developed by Hotelling. It is used in various domains (meteorology, economy, biology...). Principal component analysis is a descriptive technique; it permits the study of the relations between variables without taking account of any a priori structure. It may also be viewed as a projection tool traditionally used for dimensionality reduction. Consider a data matrix $x(k) = [x_1, x_2, \cdots, x_m]^T \in \Re^m$ consisting of *n* sample rows and *m* variable columns that are normalized to zero mean and unit variance [5].

Once a PCA model is built, a new data sample *x*, is to be tested for fault detection. It is first scaled and then decomposed as follows,

$$x = \hat{x} + \tilde{x} \tag{6}$$

where

$$\hat{x} = PP^T x \in S_P \tag{7}$$

Is the projection on the principal component subspace (PCS), S_P, and,

$$\tilde{x} = (I - PP^T)x \in S_r \tag{8}$$

Is the projection on the residual subspace (RS), S_r.

For fault detection in the new sample $\boldsymbol{x}$, a deviation in $\boldsymbol{x}$ from the normal correlation would change the projection into the subspaces, either S_P or S_r. Consequently, the magnitude of either $\tilde{x}$ or $\hat{x}$ would increase over the values obtained with the normal data.

The squared prediction error (*SPE*) indicates the difference between a sample and its projection into the *k* components retained in the model. Mathematically, the estimation error is given by

$$E = x - \hat{x} = \tilde{x} = (I - PP^T)x \tag{9}$$

And its energy as

$$SPE = \|\tilde{x}\|^2 = \|(I - PP^T)x\|^2 . \tag{10}$$

The process is considered normal if

$$SPE \le \delta^2 \tag{11}$$

Where δ^2 is a confidence limit for *SPE*.

4.2 Wavelet analysis

The wavelet Transform is defined as the integral of the signal $x(t)$ multiplied by a scaled and shifted version of a basic wavelet function $\psi(t)$, which satisfies the admissibility criteria [6],

$$c(a,b) = \int_R s(t)\frac{1}{\sqrt{a}}\psi(\frac{t-b}{a})dt \quad a \in R^+ - \{0\}, \quad b \in R \quad , \tag{13}$$

where *a* is the so-called scaling parameter, *b* is the time localization parameter. Both *a* and *b* can be continuous or discrete variables. Multiplying each coefficient by an appropriately scaled and shifted wavelet yields the constituent wavelets of the original signal. For signals of finite energy, continuous wavelet synthesis provides the reconstruction formula,

$$s(t) = \frac{1}{K_\psi}\int_R\int_{R^+} c(a,b)\frac{1}{\sqrt{a}}\psi(\frac{t-b}{b})\frac{da}{a^2}db \tag{14}$$

associated with the wavelet, which is used to define the details (high scale = low frequency content) in the decomposition, a scaling function $\psi(t)$, is used to define the approximation (low scale = high frequency content). Note that $\int\varphi(x) = 1$ while $\int\psi(x)dx = 0$.To avoid intractable computations when operating at every scale of the *CWT*, scales and positions can be chosen on a power of two, i.e. dyadic scales and positions. This defines the discrete wavelet transform (*DWT*). In this scheme, *a* and *b*are given by: $(j,k) \in Z^2 : a = 2^j$,

$$b = k2^j, \quad Z = \{0, \pm 1, \pm 2, \cdots\} \tag{15}$$

Let us define:

$$(j,k) \in Z^2 : \quad \psi_{j,k} = 2^{-j/2}\psi(2^{-j}t - k)$$

$$\phi_{j,k}(t) = 2^{-j/2}\phi(2^{-j}t - k), \tag{16}$$

A wavelet filter with impulse response *g,* which plays the role of the wavelet ψ, and a scaling filter with impulse response *h*, which plays the role of scaling function ϕ. Filters *g* and *h* are defined on a regular grid ΔZ, where Δ is the sampling period (Δ=1). Then the discrete wavelet analysis can be described mathematically as

$$C(a,b) = c(j,k) = \sum_{n\in Z} s(n)g_{j,k}(n)$$

$$a=2^j, \quad b=k2^j, \quad j \in N, k \in N \tag{17}$$

and the discrete wavelet synthesis as

$$s(t) = \sum_{j\in Z}\sum_{k\in Z} c(j,k)\psi_{j,k}(t) . \tag{18}$$

The detail at level *j* is defined as

$$D(t) = \sum_{k \in Z} c(j,k)\psi_{j,k}(t), \quad (19)$$

and the approximation at level j, $A_{j-1} = \sum_{j>J} D_j$. Obviously, the following equations hold:

$$\left.\begin{aligned} A_{j-1} &= A_j + D_j \\ s &= A_j + \sum_{j \le J} D_j \end{aligned}\right\} \quad (20)$$

In this research work, Daubechies-6 wavelet is used for vibration signal processing and analysis.

4.3 MSPCA formulation

The recent success of wavelets and multi-scale methods in analysing and diagnosing multivariate processes suggest similar successes in the investigation of fault detection methods. In this work, multi-scale principal component analysis (MSPCA) is used for fault detection and diagnosis. MSPCA simultaneously extracts both the cross correlation across the sensors (PCA approach) and the auto-correlation within a sensor (wavelet approach).Using wavelets, the individual sensor signals are decomposed into approximations and details at different scales. Contributions from each scale are collected in separate matrices, and a PCA model is then constructed to extract correlation at each scale. The multi-scale nature of MSPCA formulation makes it suitable to work with process data that are typically non-stationary and represent the cumulative effect of many underlying process phenomena, each operating at a different scale.

For the MSPCA formulation, consider a $n \times m$ data matrix X having m variables and n samples. Each of the m columns are first decomposed individually by applying a discrete wavelet transform (*DWT*). It may be noted that the same wavelet transform with the same level of decomposition L, is applied to each of the m variables. The wavelet approximation A_L from each of the m decompositions is collected in one matrix of size $m \times n / 2^L$ (as shown by the A_L solid line matrix in Fig.4).Similarly, the wavelet details (D_1 *to* D_L from each of the L levels) from each of the decompositions are collected in L corresponding matrices (as shown by the D_L dashed and D_1 dotted line matrices in Fig.4), with matrix size varying $m \times n / 2^i, \quad i = 1, 2, \cdots, L$. Thus a total of $L+1$ matrices are formed, each being represented at a different scale, and captured trends within the sensors at the corresponding scale.

The PCA is then applied to each of the $L+1$ matrices, the objective being to extract the correlation across the sensors.

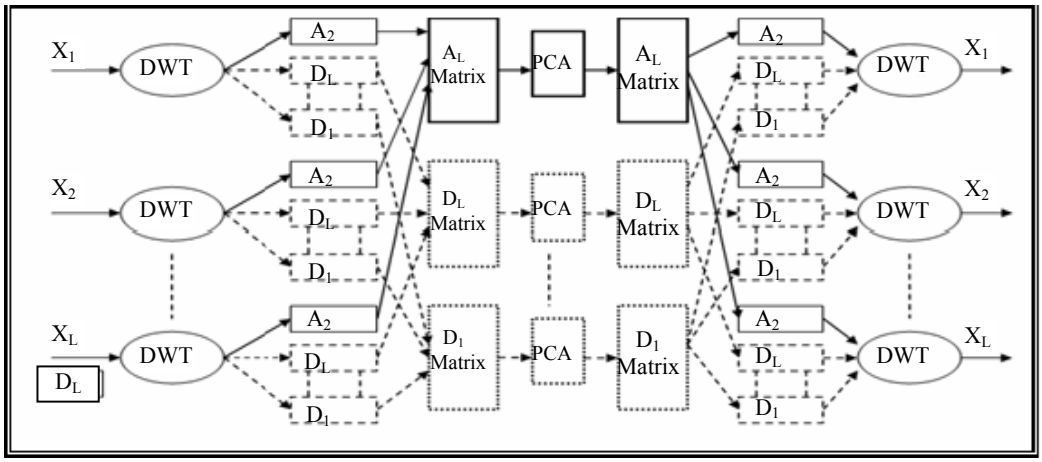

Fig. 4. Multi-scale PCA, _____ wavelet approximations mode, -------- wavelet details models

V. Fault detection with the Spectrum Energy (SE)

To compute the spectrum energy, a moving data window goes through the vibration wavelet detail coefficients shifting at a time according this expression:

$$E_w = \sum_{k=1}^{n_w} [S_w(k)]^2,$$

where $S_w(k)$ is the k^{th} spectrum coefficient within the w^{th} window and n_w is the window length. To do this detection, the spectrum energy(SE) is applied on the detail coefficients at different levels and comparing the level of this energy between the healthy and the defect bearing.

VI. Results and discussions

Experiments have been conducted on several signals of healthy and defective bearings with fault severity of different levels. However, due to limited space, results concerned with inner race faults only are considered. The acquired signals of the rotating machine in the normal operating mode and defective mode are shown in Fig.5 and 6. The simulation is done using two methods, the SPE based on the MSPCA and the spectrum Energy (SE).

The detail coefficients (D1-D4) of the healthy bearing and the inner race defects are illustrated in Fig.7, 8. With regard to the MSPCA method, it is easily seen that the presence of failure provides a very important change on the detail coefficients (D1-D4) between the healthy bearing and the defect one. The presence of failure provides also a change in the correlation between the variables indicating an abnormal situation.

In this case, the projection of the measurement vector in the residual subspace will be increased. To detect this change, the squared Prediction Error (SPE) is used.

The SPE is compared with the limit corresponding to 95% of maximal amplitude of the healthy signal in Fig. 9.

According to figures (Figs. 9-16),it is seen that the magnitude of the eigenvalue is increased in the defective case relatively with the healthy operating mode, and the defective bearing showsan SPE 95% above the limit, which is strong indication of the fault presence.

Then to detect the failures with the SE, we have calculatedthe spectrum energy of the detail coefficients (D1-D4) and the results are shown in figures (Figs.17-21). These results demonstrate that in the healthy mode operating (Fig.17) the spectrum energy of the D3 is the most important magnitude relatively to the other coefficients. However, in the defective mode, the fault is localized in the high frequencies and the spectrum energy of the D1 is the most important magnitude in relation to the other coefficients (Figs.18-21).

In conclusion, it can be said that the SPE can be used as an operational status indicator to discriminate between a safe operational mode and a defective one.

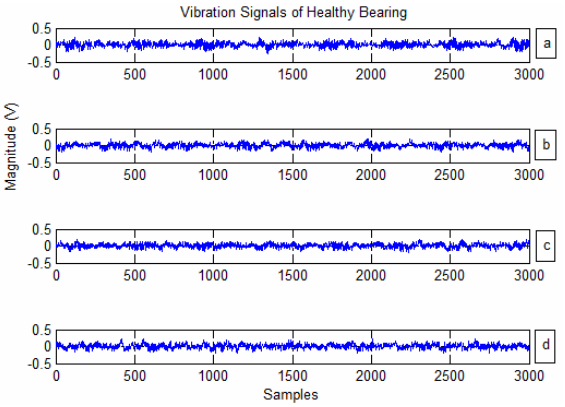

Fig. 5. Output sensors: (a, b, c, d) of healthy Bearing

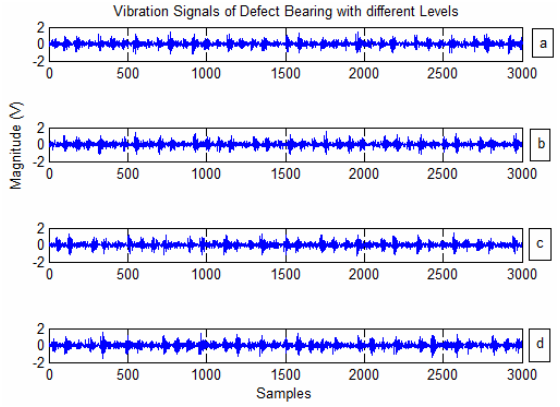

Fig. 6. Output sensors: (a, b, c, d) of defective Bearing

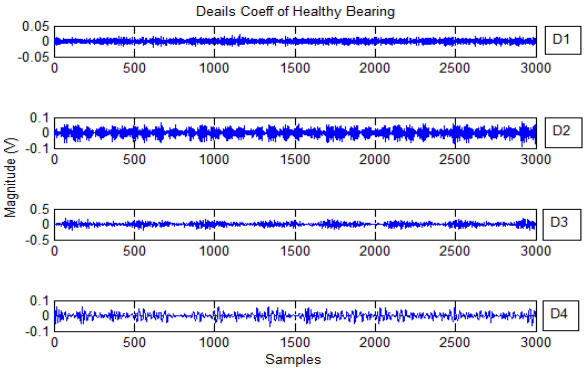

Fig. 7. Details coefficients (D1-D4)of healthy bearing

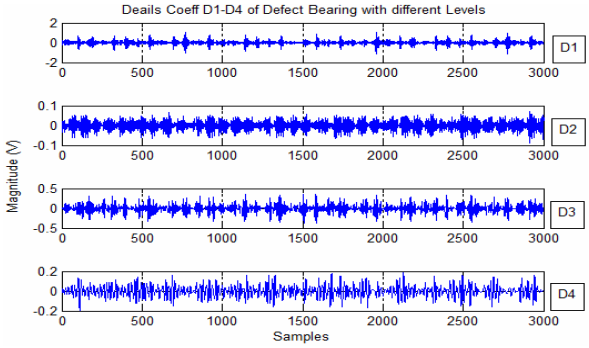

Fig. 8. Details coefficients (D1-D4) of defective bearing

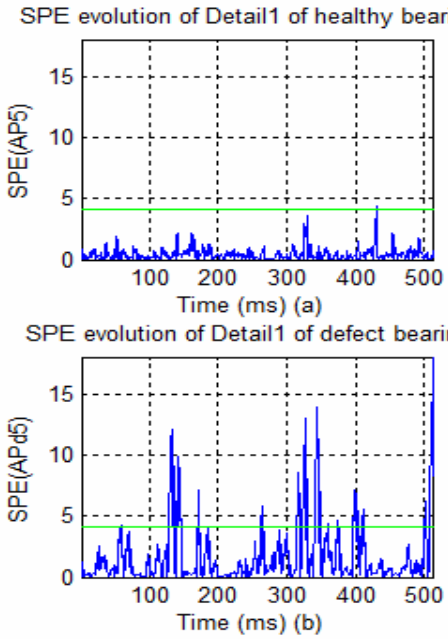

Fig. 9 SPE Evolution of D1:
a – of healthy, b – of defect bearings

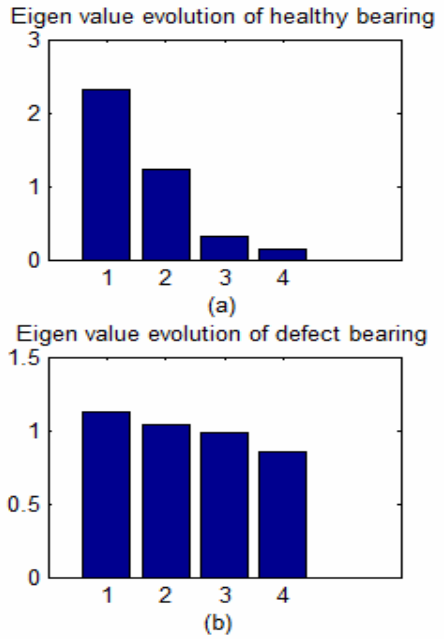

Fig. 10 Eigenvalue evolution of D1:
a – of healthy, b – of defect bearings

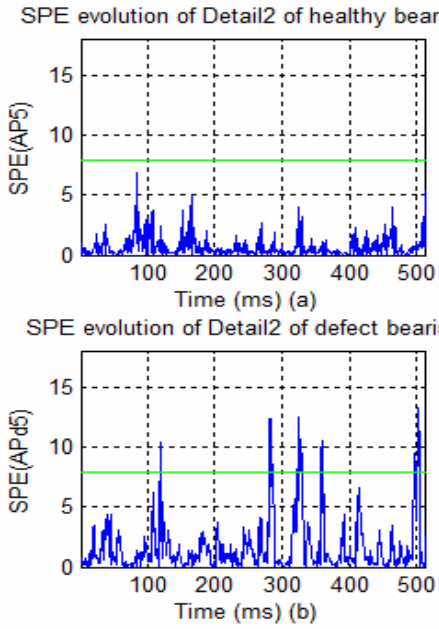

Fig.11. SPE Evolution of D2:
a – of healthy, b – of defective bearings

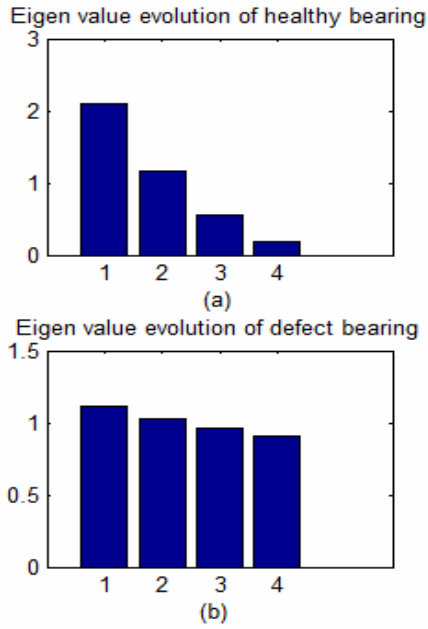

Fig.12. Eigenvalue evolution of D2:
a – of healthy, b – of defective bearings

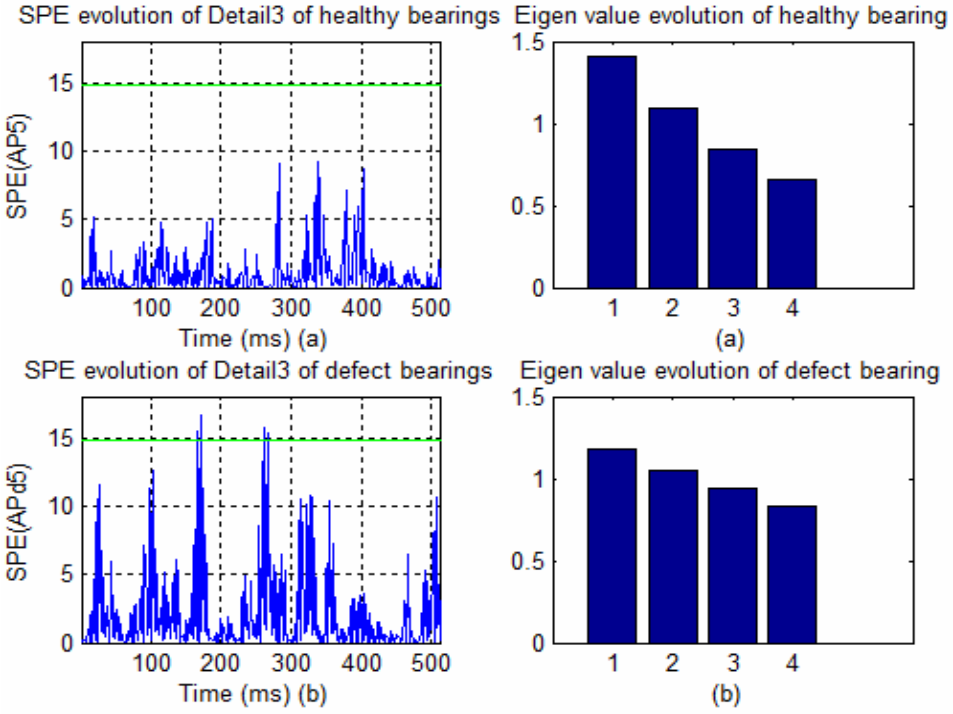

Fig.13. SPE Evolution of D3:
a – of healthy, b – of defective bearings

Fig.14. Eigenvalue evolution of D3:
a – of healthy, b – of defective bearings

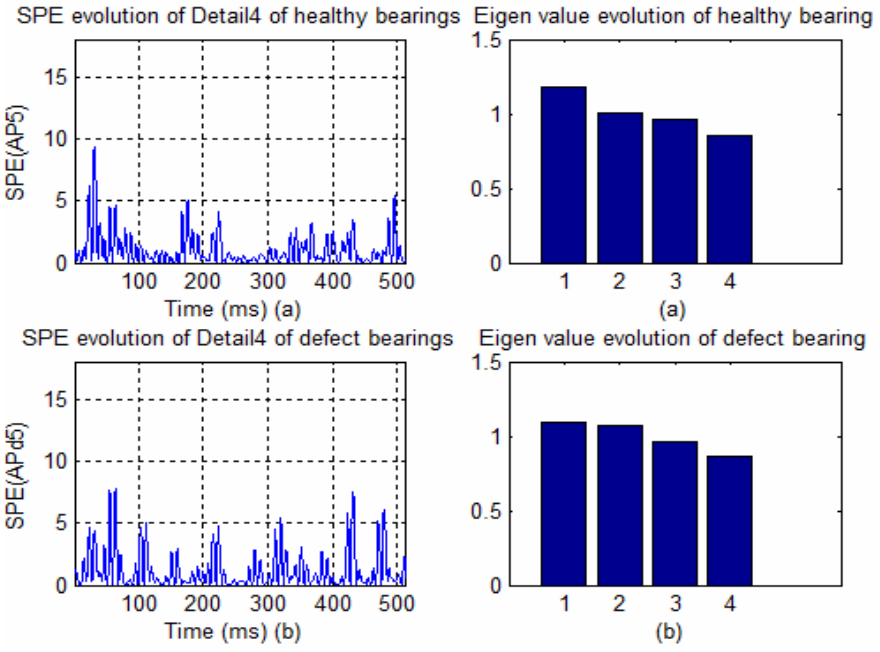

Fig. 15. SPE Evolution of D4:
a – of healthy, b – of defective bearings

Fig. 16. Eigenvalue evolution of D4:
a – of healthy, b – of defective bearings

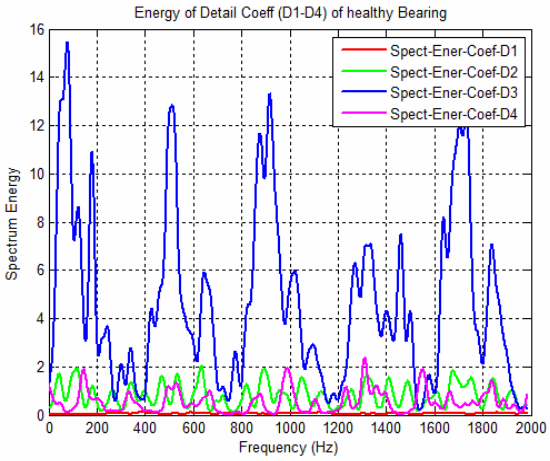

Fig. 17.Energy of detail coefficient (D1-D4) of healthy bearing

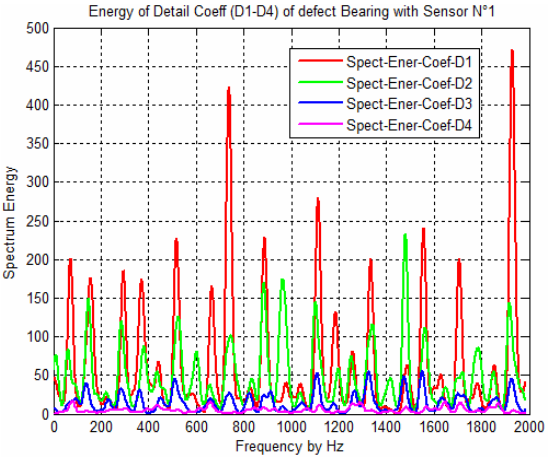

Fig. 18. Energy of detail coefficient (D1-D4) of defective bearing (sensor n°1)

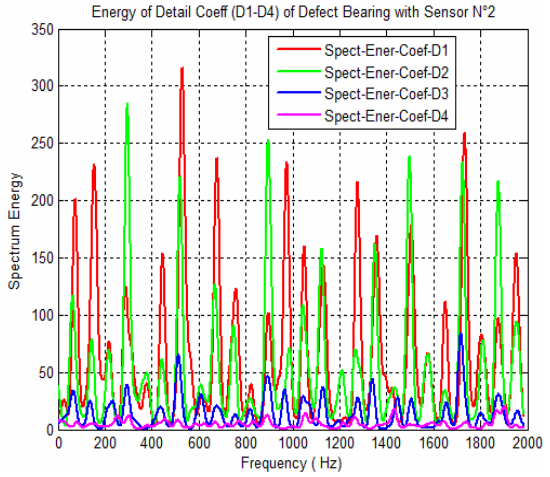

Fig. 19. Energy of detail coefficient (D1-D4) of defective bearing (sensor n°2)

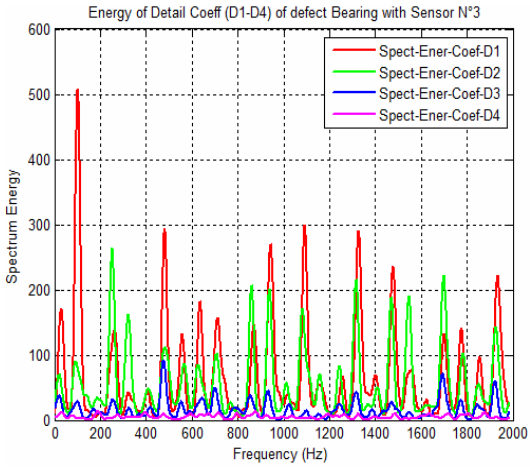

Fig. 20. Energy of detail coefficient (D1-D4) of defective bearing (sensor n°3)

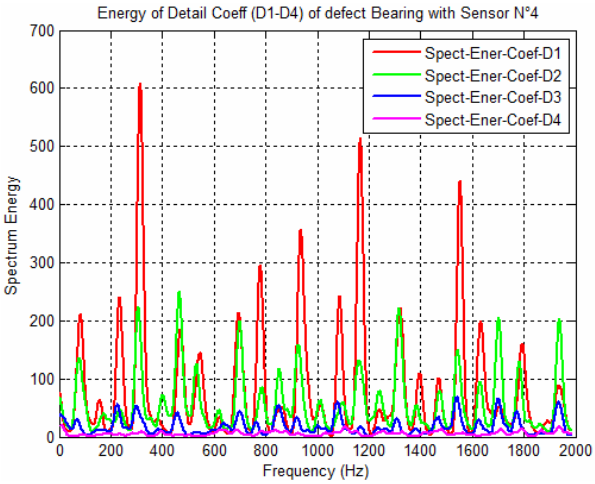

Fig. 21. Energy of detail coefficient (D1-D4) of defective bearing (sensor n° 4)

VII. Conclusion

In this work, the multi-scale principal component and spectral energy methods have been presented. To detect the presence of faults, the squared Prediction Error (SPE) and the spectrum energy of the detail coefficients are used. The SPE is compared with the limit corresponding to 95% of maximum amplitude of the healthy signal and the spectrum energy calculated from the detail coefficients. If the SPE is below the 95% limit, the sample is assumed to be in a normal operation, but if it is above, it indicates an abnormal situation. The results obtained from the SPE criteria based on the MSPCA method were confirmed by the Spectral Energy method. Then we can easily use the detail coefficient at level 1 as indicator of presence of the fault.

In fact, fault detection can be achieved by the multi-scale statistic SPE. From this technique, a considerable amount of information is acquired which can be used for the identification of different faults existing in rotating machines.

In conclusion, it can be said that SPE can be used as an operational status indicator to discriminate between a safe operational mode and a defective one.

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Reliability Tensor Model of Telecommunication Network with RED

Olexandr V. Lemeshko, Oksana Yevsyeyeva, Sergey Garkusha

Abstract — **If the user is buying a telecommunications service, he expects from the provider of a certain quality of servicing. So the delivery of telecommunications traffic must be realized with the specified quality requirements. As a rule the requirements are related to traffic rate, average delay, packet jitter, and the reliability (delivery or loss probability). The main way to meet its is finding appropriate path or multipath along which these requirements are satisfied. The multipath case is related to traffic distribution task. In this article we proposed tensor model for telecommunication network with RED and formulated analytical condition for QoS-ensuring. Satisfaction reliability of the condition guarantees that rate and requirements are be achieved at the same time. The formulated condition has invariant form that doesn't depend on AQM mechanism type.**

Index Terms — **Delivery Probability, QoS, Packet loss, RED, Reliability, Telecommunication Network, Tensor model**

I. Introduction

GUARANTEED end-to-end Quality of Service (QoS) is one of fundamental aspects of modern telecommunication network (TCN) [1]. In practice QoS ensuring is related to different traffic control features such as classification and marking, routing, shaping, policing, queuing, congestion management [2]. From viewpoint of network productivity the most effective QoS-features from the list are multipath routing as tool for load balancing and Active Queue Management (AQM) mechanisms as tool for congestion management.

In general the end-to-end QoS requires guaranteeing on multiple QoS-parameters, such as rate, average delay, packet jitter, and the reliability (delivery or loss probability) at the same time. As result QoS ensuring is complex and difficult task that needs appropriate mathematical models and algorithms. Currently within the existing technological traffic control means (protocols and mechanisms) the routing and AQM problems are solved apart by using low-level (from viewpoint of their theoretical justification) heuristic models and schemes [3] – [4].

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Therefore an important scientific and engineering problem is developing sufficient mathematical models that can formalize the process of QoS ensuring within solving the traffic control task with taking into account multipath routing and AQM mechanisms on routers. In this regard, approach based on the tensor representation of the telecommunication network deserves attention. This mathematical tool has already proven itself to provide effective holistic and multi-aspect description of telecommunication network. In [5] – [6] tensor model of TCN enables to obtain analytical conditions for satisfaction rate and delay requirements at same time under multipath routing.

Providing a required level of reliability of traffic delivery is related to using measurements such as the probability of timely delivery of packet, the probability of authentic delivery of packet, the probability of failure-free operation, availability factor, etc. Reference [7] develops reliability tensor model of TCN in terms of the probability of failure-free operation. In this article we'll focus on the probability of packet loss (IP packet Loss Ratio, IPLR), which is one of the key characteristics of Network Performance [8].

II. Tensor Model of the Telecommunication Network with RED

In order to develop tensor model of TCN we'll use a technique based on the generalization postulates of G. Kron [9]. According to a preliminary postulate in the first phase of development behavior equation for a single element of the system should be written. Let us choose link as single element of telecommunication network. Then we'll consider the network as a set of connected in a certain way (within a certain structure) links.

It is known that the delivery of the packet in the link and the loss of the packet form a complete group of events, i.e.

$$p = 1 - p_l, \tag{1}$$

where p – the probability of packet delivery; p_l – the probability of packet loss.

In general, the causes of a packet loss can be different, for example, the signal's distortion, coding errors, incorrect addressing, a large network delay and expiration of TTL of the packet. But the main reason of packet loss in transport network is related to a buffer overflow and packet drops, i.e. mechanisms of passive and active queue management. At present, most widely applicable queue management mechanisms in the packet-switched networks are Random Early Detection (RED) and its different modifications [2], [4].

RED and its modifications belong to AQM mechanisms where dropping of packets from queue can happen before buffer overflow. Under RED, discard function p_l is linear function of the average length of the queue q

$$p_l = \frac{q - \Theta_{min}}{\Theta_{max} - \Theta_{min}} \cdot \frac{1}{\delta}, \quad (2)$$

where q – actual size of the queue (number of packets in queue); Θ_{min} – minimum threshold (if the average queue falls below this minimum threshold then no packets are discarded); Θ_{max} – maximum threshold (if the falls above this maximum threshold all packets are discarded); δ – mark probability denominator.

Then delivery probability for link under RED is

$$p = 1 - \frac{q - \Theta_{min}}{\Theta_{max} - \Theta_{min}} \cdot \frac{1}{\delta}. \quad (3)$$

The average length of queue q is function of traffic intensity transmitted through the router (link) for the formalization of which we will use the results of queuing theory as one possible way of its analytical representation. By using queuing system $M/M/1/N$ this quantity can be represented as [10]

$$q = \frac{\rho}{1-\rho} - \frac{(N+1)\rho^{N+1}}{1-\rho^{N+1}} - \rho. \quad (4)$$

where $N = \Theta_b + 1$; Θ_b – buffer size; $\rho = \frac{\lambda}{\varphi}$ – utilization of the link; φ – capacity of the link; λ – traffic rate in the link.

Note, as well as in the case of the functional equation for a single network element, the estimated average queue length can be obtained not only by using the queuing theory, but also by using other mathematical tools such as Markov processes, empirical methods, etc.

Let us add a sliding index i for indicating the number of the link, then the functional equation for reliability of the i^{th} link can be written as

$$p_i^{(v)} = 1 - \frac{\left(\frac{\rho_i}{1-\rho_i} - \frac{(N_i+1)\rho_i^{N_i+1}}{1-\rho_i^{N_i+1}} - \rho_i \right) - \Theta_{min}}{\Theta_{max} - \Theta_{min}} \cdot \frac{1}{\delta}, \quad (5)$$

where $p_i^{(v)}$ – the probability of packet delivery through i^{th} link, $i = \overline{1,n}$; (v) – mute index (indicates that the link belongs to set of edges V in graph model of network) [11]; ρ_i – utilization of the i^{th} link; n – number of link in the network.

The system of equations (5) describes separated network links. Before turning the system of equations into one tensor equation we must be sure that every object from the system (5) has tensor nature. References [5] – [6] show tensor nature of some network parameters (metrics). It is known that additive metrics such as delay, jitter are covariant tensors but metrics satisfying conservation constraint, for instance, traffic intensity or rate, are contravariant tensors.

The probability of packet delivery is multiplicative metric, i.e.

$$p^{(path)} = \prod_{i:v_i \in path} p_i^{(v)}.$$

Let us turn the multiplicative metric into the additive

$$\mathbf{log}_a(p^{(path)}) = \sum_{i:v_i \in path} \mathbf{log}_a(p_i^{(v)}).$$

Then (5) takes the form

$$\mathbf{log}_a(p_i^{(v)}) = \left[\frac{1}{\lambda_{(v)}^i} \times \right.$$
$$\left. \times \mathbf{log}_a \left(1 - \frac{\left(\frac{\rho_i}{1-\rho_i} - \frac{(N_i+1)\rho_i^{N_i+1}}{1-\rho_i^{N_i+1}} - \rho_i \right) - \Theta_{min}}{\Theta_{max} - \Theta_{min}} \cdot \frac{1}{\delta} \right) \right] \lambda_{(v)}^i \quad (6)$$

or

$$P_v = \Theta_v \Lambda_v, \quad (7)$$

where N_i and $\lambda_{(v)}^i$ belong to i^{th} link; P_v – vector of reduced (turned into additive form) probability of packet delivery with elements $\mathbf{log}_a(p_i^{(v)})$; Θ_v – diagonal matrix with elements

$$\theta_{ii}^{(v)} = \frac{1}{\lambda_{(v)}^i} \mathbf{log}_a \left(1 - \frac{\left(\frac{\rho_i}{1-\rho_i} - \frac{(N_i+1)\rho_i^{N_i+1}}{1-\rho_i^{N_i+1}} - \rho_i \right) - \Theta_{min}}{(\Theta_{max} - \Theta_{min})\delta} \right). \quad (8)$$

Equation (7) can be interpreted as a projection of the following invariant (tensor) equation in the coordinate system (CS) of edges (type v)

$$\mathbf{P} = \mathbf{\Theta\Lambda}, \tag{9}$$

where $\mathbf{P}$ – univalent covariant tensor of the reduced probability of packet delivery; $\mathbf{\Lambda}$ – univalent contravariant tensor of traffic intensity; $\mathbf{\Theta}$ – divalent covariant tensor acting as a metric tensor.

Equation (9) can be written as

$$\mathbf{\Lambda} = \mathbf{XP}, \tag{10}$$

where $\mathbf{X}$ – divalent contravariant metric tensor, whose projection in the CS of edges is $X_v = [\Theta_v]^{-1}$.

Note that coordinate system of edges considers the network as a set of separated links, i.e. set of single edges.

Thus, probability tensor model of TCN can be reduced to an invariant tensor equation (9), where coordinates of the divalent covariant tensor $\mathbf{\Theta}$ (8) in the CS of edges are functions of the discarding parameters ($\Theta_{\min}$, $\Theta_{\max}$, δ), the size of buffer (Θ_b), the capacities of the links (φ_i), and the intensities of the traffic transmitted through the routers ($\lambda^i_{(v)}$).

III. Formulation of Condition for Ensuring Required Reliability of Service

In order to derive the condition for ensuring quality in terms of reliability we'll use orthogonal representation of the tensor model of TCN (9) – (10) in CS of circuits and pairs of nodes. This CS considers the network as a set of circuits π and node pairs η, where total dimension of CS is equal to n. Then the projections of tensors of traffic intensity $\mathbf{\Lambda}$ and the reduced probability of delivery $\mathbf{P}$ in this coordinate system can be represented by the following vectors:

$$\Lambda_{\pi\eta} = \begin{Vmatrix} \Lambda_\pi \\ -- \\ \Lambda_\eta \end{Vmatrix}, \quad \Lambda_\pi = \begin{Vmatrix} \lambda^1_{(\pi)} \\ \vdots \\ \lambda^j_{(\pi)} \\ \vdots \\ \lambda^\mu_{(\pi)} \end{Vmatrix}, \quad \Lambda_\eta = \begin{Vmatrix} \lambda^1_{(\eta)} \\ \vdots \\ \lambda^j_{(\eta)} \\ \vdots \\ \lambda^\phi_{(\eta)} \end{Vmatrix}, \tag{11}$$

$$P_{\pi\eta} = \begin{Vmatrix} P_\pi \\ -- \\ P_\eta \end{Vmatrix}, \quad P_\pi = \begin{Vmatrix} p^{(\pi)}_1 \\ \vdots \\ p^{(\pi)}_j \\ \vdots \\ p^{(\pi)}_\mu \end{Vmatrix}, \quad P_\eta = \begin{Vmatrix} p^{(\eta)}_1 \\ \vdots \\ p^{(\eta)}_j \\ \vdots \\ p^{(\eta)}_\phi \end{Vmatrix}, \tag{12}$$

where $\Lambda_{\pi\eta}$, $P_{\pi\eta}$ – n-dimensional vectors that are projections of tensors $\mathbf{P}$ and $\mathbf{\Lambda}$ in CS of circuits and node pairs; Λ_π, P_π – μ-dimensional subvectors related to circuits in network, $\mu = n - m + 1$; m – number of nodes in the network; Λ_η, P_η – ϕ-dimensional subvectors related to node pairs in network, $\phi = m - 1$.

Note that circuit components $\lambda^j_{(\pi)}$ and $p^{(\pi)}_j$ from subvectors Λ_π and P_π are related to circuits in a network. So in order to eliminate loops in routes we must satisfy the next condition

$$P_\pi = 0. \tag{13}$$

The components of subvectors Λ_η and P_η show traffic intensity and the reduced probability of delivery for different pairs of nodes in a network. Then according flow conservation law for every transit nodes value λ^j_η must be zero:

$$\Lambda_\eta = \left\| \lambda^1_{(\eta)} \quad 0 \quad \dots \quad 0 \right\|^t, \tag{14}$$

where $\lambda^1_{(\eta)}$ – traffic intensity between end points which form first pair of nodes.

In accordance with the second generalization postulate of G. Kron [9] tensor equations (9) and (10) have the same form in every the coordinate system, i.e. in CS of circuits and node pairs tensor equation (10) takes the form

$$\Lambda_{\pi\eta} = X_{\pi\eta} P_{\pi\eta}, \tag{15}$$

where $X_{\pi\eta}$ – projection of tensor $\mathbf{X}$ in CS of circuits and node pairs.

According to laws of tensor calculus projections of tensors $\mathbf{P}$, $\mathbf{\Lambda}$ and $\mathbf{X}$ in the CS of circuits and node pairs (type $\pi\eta$) and in the CS of edges (type v) are related as follows

$$P_v = A\ P_{\pi\eta}, \tag{16}$$

$$\Lambda_v = C\,\Lambda_{\pi\eta}, \tag{17}$$

$$X_v = C X_{\pi\eta} C^t, \tag{18}$$

$$X_{\pi\eta} = A^t X_v A. \tag{19}$$

where A and C – matrices of co- and contravariant transformation of coordinates when transition from CS of circuits and node pairs to CS of edges.

Using (11) – (12) we can represent (15) in next form

$$\begin{Vmatrix} \Lambda_\pi \\ --- \\ \Lambda_\eta \end{Vmatrix} = \begin{Vmatrix} X^{\langle 1 \rangle}_{\pi\eta} & | & X^{\langle 2 \rangle}_{\pi\eta} \\ --- & + & --- \\ X^{\langle 3 \rangle}_{\pi\eta} & | & X^{\langle 4 \rangle}_{\pi\eta} \end{Vmatrix} \cdot \begin{Vmatrix} P_\pi \\ --- \\ P_\eta \end{Vmatrix}, \tag{20}$$

where $\left\| \begin{matrix} X_{\pi\eta}^{\langle 1\rangle} & | & X_{\pi\eta}^{\langle 2\rangle} \\ --- & + & --- \\ X_{\pi\eta}^{\langle 3\rangle} & | & X_{\pi\eta}^{\langle 4\rangle} \end{matrix} \right\| = X_{\pi\eta}$, $X_{\pi\eta}^{\langle 1\rangle}$, $X_{\pi\eta}^{\langle 4\rangle}$ – square $\mu\times\mu$ and $\phi\times\phi$ submatrices, respectively; $X_{\pi\eta}^{\langle 2\rangle}$ – $\mu\times\phi$ submatrix, $X_{\pi\eta}^{\langle 3\rangle}$ – $\phi\times\mu$ submatrix.

Then from (20) and according (13) we have

$$\Lambda_\eta = X_{\pi\eta}^{\langle 4\rangle} P_\eta . \qquad (21)$$

Further we will consider vectors Λ_η and P_η as $\Lambda_\eta = \left\| \begin{matrix} \lambda_{(\eta)}^1 \\ --- \\ \Lambda_{\eta-1} \end{matrix} \right\|$, $P_\eta = \left\| \begin{matrix} p_1^{(\eta)} \\ --- \\ P_{\eta-1} \end{matrix} \right\|$, where $p_1^{(\eta)}$ – reduced probability of traffic delivery between end points which form first pair of nodes. Then (21) can be turned into

$$\left\| \begin{matrix} \lambda_{(\eta)}^1 \\ --- \\ \Lambda_{\eta-1} \end{matrix} \right\| = \left\| \begin{matrix} X_{\pi\eta}^{\langle 4,1\rangle} & | & X_{\pi\eta}^{\langle 4,2\rangle} \\ --- & + & --- \\ X_{\pi\eta}^{\langle 4,3\rangle} & | & X_{\pi\eta}^{\langle 4,4\rangle} \end{matrix} \right\| \cdot \left\| \begin{matrix} p_1^{(\eta)} \\ --- \\ P_{\eta-1} \end{matrix} \right\|, \qquad (22)$$

where $\left\| \begin{matrix} X_{\pi\eta}^{\langle 4,1\rangle} & | & X_{\pi\eta}^{\langle 4,2\rangle} \\ --- & + & --- \\ X_{\pi\eta}^{\langle 4,3\rangle} & | & X_{\pi\eta}^{\langle 4,4\rangle} \end{matrix} \right\| = X_{\pi\eta}^{\langle 4\rangle}$, $X_{\pi\eta}^{\langle 4,1\rangle}$ – the first element of the matrix $X_{\pi\eta}^{\langle 4\rangle}$.

From (14) and (22) we obtain

$$\lambda_{(\eta)}^1 = \left(X_{\pi\eta}^{\langle 4,1\rangle} - X_{\pi\eta}^{\langle 4,2\rangle} \left[X_{\pi\eta}^{\langle 4,4\rangle} \right]^{-1} X_{\pi\eta}^{\langle 4,3\rangle} \right) p_1^{(\eta)} . \qquad (23)$$

Elements $\lambda_{(\eta)}^1$ and $p_1^{(\eta)}$ are related to pair source-destination and in general can include requirements for traffic intensity (rate) and the reduced probability of delivery (reliability) for this pair, i.e. $\lambda_{(\eta)}^1 = \lambda^{\langle req\rangle}$, $p_1^{(\eta)} = p_{\langle req\rangle}$, $p_{\langle req\rangle} = \mathbf{log}_a \left(1 - P_{IPLR}^{\langle req\rangle}\right)$, $P_{IPLR}^{\langle req\rangle}$ – required value of IPLR.

Then finally we have the following inequality

$$\lambda^{\langle req\rangle} \geq \left(X_{\pi\eta}^{\langle 4,1\rangle} - X_{\pi\eta}^{\langle 4,2\rangle} \left[X_{\pi\eta}^{\langle 4,4\rangle} \right]^{-1} X_{\pi\eta}^{\langle 4,3\rangle} \right) p_{\langle req\rangle} , \qquad (24)$$

which is a formalization of the condition for ensuring the required quality of service between a given pair of recipients from reliability point of view. It is assumed that this condition can be placed into dynamic or static model of TCN for solving traffic control (engineering) problem in networks with guaranteed QoS.

IV. Example of the Solution of the QoS- Ensuring Problem with Rate and Reliability Requirements

Let us make an example of solving QoS-ensuring problem with two required parameters (transmission rate and the probability of packet delivery) in environment of multipath routing and active queue management mechanism such as RED. The solving QoS-ensuring problem is related to traffic distribution under which given QoS-requirements will be satisfied. Fig. 1 shows example of network where capacity φ_i for every link is known (Table I). For given pair source-destination we will find set of routes such as total for traffic rate (intensity) from source to destination will be not less than $\lambda^{\langle req\rangle} = 535$ 1/s (in packets per second) and result loss will be not more than $P_{IPLR}^{\langle req\rangle} = 0{,}03$ ($p_{\langle req\rangle} = \mathbf{log}_2(0{,}97) = -0{,}0439$). To simplify the problem, assume parameters of mechanism RED on all nodes are the same: $\Theta_{\mathbf{min}} = 5$ and $\Theta_{\mathbf{max}} = 40$ packets, $\delta = 10$, which correspond to the recommended parameters.

Numerical results that satisfy the condition (24) and given QoS-requirements are shown into Table I and in Fig. 2. According to the results for servicing traffic between nodes 1 (source) and 6 (destination) at given rate $\lambda^{\langle req\rangle}$ and with given IPLR $P_{IPLR}^{\langle req\rangle}$ we need use four paths that are shown in Fig. 1 and into Table II.

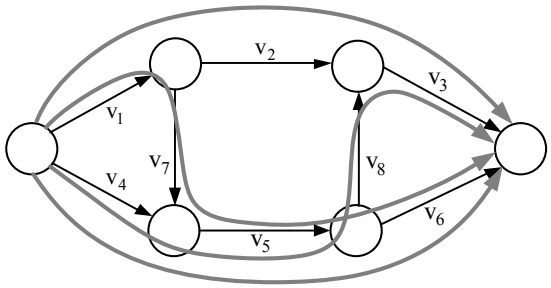

Fig. 1. Example of network structure and obtained set of paths

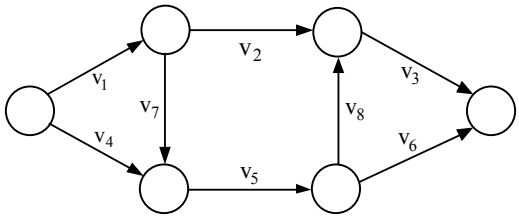

Fig. 2. Result traffic distribution between links that satisfy given QoS-requirements. Values near every link show (top-down) capacity, traffic intensity and the probability of delivering through the link

TABLE I
RESULT TRAFFIC DISTRIBUTION AS SOLUTION OF QOS-ENSURING PROBLEM

Number of the link (edge) i	Capacity of the link φ_i, 1/s	Traffic intensity in the link $\lambda^i_{(v)}$, 1/s	Reduced probability of delivery $\log_2(p_i^{(v)})$	Probability of delivery in the link $p_i^{(v)}$	Probability of loss in the link $1-p_i^{(v)}$
1	445	401	-0,0116	0,9920	0,0080
2	282	265	-0,0268	0,9816	0,0184
3	432	381	-0,0055	0,9962	0,0038
4	147	134	-0,0155	0,9893	0,0107
5	292	270	-0,0195	0,9866	0,0134
6	172	154	-0,0089	0,9939	0,0061
7	155	136	-0,0039	0,9973	0,0027
8	133	116	-0,0034	0,9977	0,0023

TABLE II
SET OF USED ROUTES AND PROBABILITY OF DELIVERY THROUGH ITS

Path	Traffic intensity through path, 1/s	Probability of delivery through path
(v_1, v_2, v_3)	≈265	$(0{,}992 \cdot 0{,}9816 \cdot 0{,}9962) \approx 0{,}97$
(v_1, v_5, v_6, v_7)	≈136	$(0{,}992 \cdot 0{,}9866 \cdot 0{,}9939 \cdot 0{,}9973) \approx 0{,}97$
(v_4, v_5, v_6)	≈18	$(0{,}9893 \cdot 0{,}9866 \cdot 0{,}9939) \approx 0{,}97$
(v_3, v_4, v_5, v_8)	≈116	$(0{,}9962 \cdot 0{,}9893 \cdot 0{,}9866 \cdot 0{,}9977) \approx 0{,}97$

Thus, the obtained solution, firstly, meets the specified rate and reliability (packet loss) requirements, and secondly, provides not only desired, but the same probability of delivery (loss) through all traffic routes.

V. CONCLUSION

Thus, the problem of traffic control with QoS-ensuring requires an adequate mathematical model of the telecommunication network that take into account the QoS requirements, on the one hand, and the structural and functional features of the TCN and characteristics of traffic, on the another hand. Such contradictory requirements can be satisfied within tensor approach, which has been demonstrated in this paper. The obtained formalization of the condition for ensuring the required reliability of service in networks takes into account characteristics of traffic, the parameters of the active queue management mechanisms, the structural properties of the network and focuses on the multipath transmitting. The condition (24) was formulated from invariant tensor equations and has invariant form that doesn't depend on AQM mechanism type. The parameters of AQM affect numerical values of the projections of the metric tensor, and doesn't affect the form of the condition (24). This distinctive feature allows to apply the condition (24) in the network not only with RED, but with other mechanisms of active queue management.

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Query Optimization Based on Time Scheduling Approach

Wajeb Gharibi, Ayman Mousa

Abstract – **Distributed database systems suffer from many difficulties. The most common difficulty is the environment where such systems mostly are running on unpredictable and volatile environments. So it is difficult to produce efficient database query optimization based on information available at compilation time. The performance of re-optimization techniques which are used by many systems suffers from problems. This paper attempts to reduce query re-optimization by executing a set of simple predefined queries in predefined time scheduling approach to collect estimates of statistics at runtime. For this purpose, a timer object with adaptive query processing systems is proposed. Experimental result is given to demonstrate the performance of real queries. This result shows significant performance improvements is obtained compared with other traditional approaches when the proposed object timer is used.**

Index Terms – **Query optimization, adaptive query processing, query reoptimization, distributed database**

I. Introduction

RESEARCH in distributed database systems has popularized the mediator/wrapper architecture. The mediator provides a uniform interface to query heterogeneous data sources while wrappers map the uniform interface into the data source interfaces [11]. In this context, processing a query consists in sending sub-queries to data source wrappers, and then integrating the sub-query results at the mediator level to produce the final response. One of the key reasons for the success of relational database technology is the use of declarative languages and query optimization. The user can just specify what data needs to be retrieved and the database takes over the task of finding the most efficient method of retrieving that data. It is the job of the query optimizer to evaluate alternative methods of executing a query, and selecting the best alternative [2].

Several techniques have been proposed to improve traditional query optimization. These techniques include better statistics [12], new algorithms for optimization, and adaptive architectures for execution [3]. A very promising technique in this direction is reoptimization, where the optimization and the execution stages of processing a query are interleaved, possibly multiple times, over the running time of the query [6][7][14]. Current re-optimizers take a reactive approach to re-optimization. In this case use a traditional optimizer is used to generate a plan, then track statistics and respond to estimation errors and resulting sub-optimality detected in the plan during execution. Reactive reoptimization is limited by its use of an optimizer that does not incorporate issues affecting reoptimization, and suffers from several shortcomings. Also proactive reoptimization approach [5] is used during optimization to generate robust and switch able plans and it is used random-sample processing for every query execution, consequently it is suffered from some negative points affecting from reoptimization process that mention in section III.

This paper presents query optimization based on time scheduling approach to reduce query reoptimization. For this purpose, we added a timer object with adaptive query processing systems to handle the problems with effect reoptimization. A timer object built to execute a set of simple predefined queries in predefined time scheduling to collect estimates of statistics about the database quickly, accurately, and efficiently at runtime. When the timer object fires (multiple times) executes a set of simple queries that were specify, and the amount of time specify between executions of the timer object perform execution of the real queries. Finally we present simulation experimental that demonstrated our anew approach results in significant improvements on the performance of the real queries.

The remainder of this paper is organized as follows. Section II discusses related work to query reoptimization techniques. Section III focuses on the problems with reactive reoptimization and the problems with proactive reoptimization. Section IV shows time scheduling approach. Section V a typical example with simulation results. Finally section VI presents conclusions.

II. Related Work

In the most cases the distributed database environment is running on unpredictable and volatile environments. So it is difficult to produce efficient database query optimization based on information available at compilation time. A solution to this problem is to exploit information that becomes available at query runtime and adapt the query plan to changing environmental conditions during execution. This section presents adaptive query plan reoptimization techniques which were used to modify query plan dynamically at runtime.

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Mid-query Re-optimization [6], dealt with mid-estimated intermediate result sizes in a lazy-evaluation way, by extending a traditional execution system so that it could re-invoke the optimizer after completion of any pipelined segment of the initial plan. Their system inserts statistical monitors where they incur low overhead but provide information about when re-optimization is useful.

Query Scrambling [17], was developed specifically to cope with unexpected delays that arise when processing distributed queries in a wide-area network. With Query Scrambling, a query is initially executed according to a plan generated by query optimizer. If, a significant performance problem is detected during the execution, the query plan is modified on the fly. Query Scrambling uses two basic techniques to cope with unexpected delays rescheduling and operator synthesis.

Tukwila system [8], addressing adaptiveness in data integration environment. Adaptiveness is introduced at two levels: In the first level, Adaptiveness is deployed by annotating initial query plans by ECA rules (event-condition-action). These rules check some conditions when certain events occur and subsequently trigger the execution of some actions. For the second level of adaptiveness, two operators are used: dynamic collector operator dynamically chooses relevant sources when a union involves data from possibly overlapping or redundant sources, and the double pipelined hash join operator is a symmetric and incremental join.

Eddies algorithm [3], an eddy encapsulates the ordering of operators by dynamically routing tuples through them. The idea is that there are times during the processing of a binary operator (e.g., join, union) when it is possible to modify the order of the inputs without modifying any state in the operator.

Convergent Query Processing [18], present a logical query optimization framework and a set of adaptive techniques, In high level, it is similar to several previous methods, during execution do monitor the costs of operations and size of intermediate results, if the plan is poor, must replace it with one that is expected to perform better.

Progressive query optimization (POP) [9], provides a plan "insurance policy" by lazily triggering re-optimization in the midst of query execution whenever cardinality estimation errors indicate that the QEP might be sub-optimal. It does this by adding one or more checkpoint operators (CHECK), which compare the optimizer's cardinality estimates with the actual number of rows processed thus far, and trigger reoptimization if a pre-determined threshold on the error is exceeded. Note, the merger POP technique and use a Timer Object will be give high performance in the execution of the queries.

Proactive re-optimization approach [5] incorporates three techniques:

- Bounding boxes are computed around estimates of statistics to represent the uncertainty in these estimates.
- The bounding boxes are used during optimization to generate robust and switchable plans that minimize the need for reoptimization and the loss of pipelined work.
- Random-sample processing is merged with regular query execution to collect statistics at run-time.

Note, not use a Timer Object with this approach because the system will be poor performance in the execution of the queries. Fig.1 presents related a Timer Object with adaptive query plan reoptimization techniques.

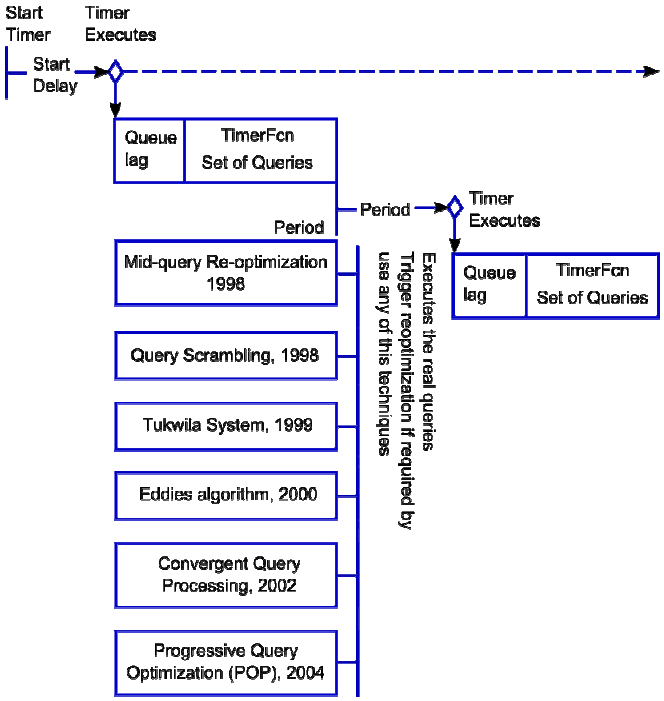

Fig.1 Timer Object with query re-optimization techniques

III. Problems With Reactive And Proactive Reoptimization

The query optimizers use a plan-first execute-next approach; the optimizer enumerates plans, computes the cost of each plan, and picks the plan with lowest cost [16]. Current re-optimizers take a reactive approach to reoptimization, they use a traditional optimizer to generate a plan, and then track statistics and respond to estimation errors and resulting sub-optimality detected in the plan during execution. Reactive reoptimization is limited by its use of an optimizer that does not incorporate issues affecting re-optimization, and suffers from at least three shortcomings:

- The optimizer may pick plans whose performance depends heavily on uncertain statistics, making re-optimization very likely.
- The partial work done in a pipelined plan is lost when reoptimization is triggered and the plan is changed.
- The ability to collect estimates statistics quickly and accurately during query execution is limited. Consequently, when reoptimization is triggered, the optimizer may make new mistakes, leading potentially to thrashing.

The proactive reoptimization approach [5] used during optimization to generate robust and switch-able plans and it is used random-sample processing for every query execution, consequently it is suffer from some negative points affecting from reoptimization process:

− It defines a robust plan as one that is “near optimal" but gives no formulae for comparing a robust plan with an optimal one. How close is good enough?

− The idea of robust plans is very appealing, but this approach gives little evidence. Switchable plans appear to be more promising, although they do not always allow the reuse of work.

− Every execution query, executes random-sample tuples which is merged with regular query execution to collect statistics, hence incur high overhead. And before this during optimization generate robust and switchable plans to select execution plan this making delay.

− This approach would have been much easier to understand if they had gone ahead and drawn detailed bounding boxes for each of their examples. And it was difficult to keep track of them without drawing a box in the margins and marking it.

IV. TIME SCHEDULING APPROACH

Query optimization based on time scheduling approach is aimed to reduce query reoptimization. This approach executes a set of simple predefined queries in predefined time scheduling to collect estimates statistics about the database quickly, accurately, and efficiently at runtime. For this purpose, a Timer Object [10] incorporate with adaptive query processing systems to handle the problems with reactive and proactive reoptimization approaches that were as mentioned in section III. When the amount of time specified by the timer object elapses (much time elapses before the timer fires) and the timer object fires (multiple times to execute a timer object) executes a set of simple queries that were specify, and the amount of time specify (the period time) between executions of the timer object perform execution of the real queries. Fig.2 illustrated architecture a Timer Object with adaptive query processing systems (AQP) [4].

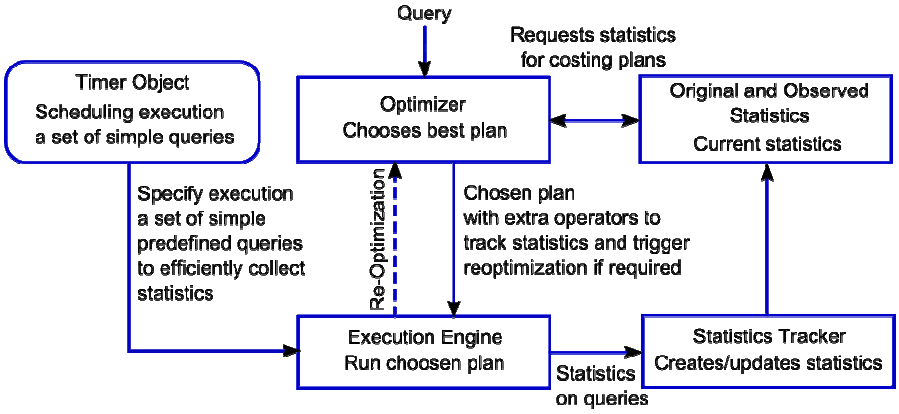

Fig.2 Architecture a Timer Object with AQP.

Every query in a set of simple queries is select primary key field (numeric field, because this field is very small size take littleness execution time) from all tables in database to efficiently collect statistics on the execution environment such as CPU workload, network traffic, available memory and resource availability. The different query execution plans share the same system statistics, predictions, and on the estimation of query characteristics (e.g. the data selectivities of operators are computed on the fly and the number of the tuples in every table).

Database administrator invokes these simple queries by running a timer objects multiple times every day on period specify to collect new estimates statistics and to bring existing ones up-to-date statistics continuous at runtime. The following general configuration the simple predefined queries (e.g. SQL language):

Q1: SELECT Fieldname (primary key or numeric field)
FROM Tablename1
Q2: SELECT Fieldname (primary key or numeric field)
FROM Tablename2
⋮
Qn: SELECT Fieldname (primary key or numeric field)
FROM Tablenamen

A. Use a Timer Object

− Create a timer object;

− Specify the set of the queries will be executed when the timer object fires, and control other aspects of the timer object behavior;

− Start and stop the timer object;

− Delete the timer object when done the work.

B. Timer Object Execution Modes

The timer object supports several execution modes that

determine how it schedules the timer object function (TimerFcn, it is the some of commands or file to execute when the timer fires) for execution. Specify the execution mode a timer object function Once or Multiple Times [10].

1) Executing a Timer Object Function Once

To execute a timer object function once, set the execution mode property to 'Single Shot'. This is the default execution mode. In this mode, the timer object starts the timer, after the time period specified (much time elapses before the timer fires), adds the timer (TimerFcn) to the execution queue. When the timer function finishes, the timer stops. Fig.3 illustrates the parts of the timer object execution for a single shot execution mode.

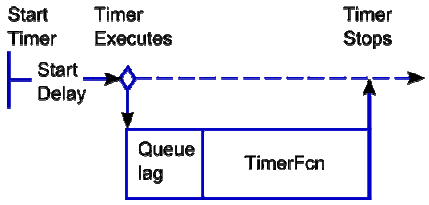

Fig. 3. Timer Object execution (Single Shot Execution Mode)

The shaded area is shown in the Fig.3 where the label queue lag, represents the indeterminate amount of time between when the timer adds a timer function to the execution queue and when the function starts executing. The duration of this lag is dependent on what other processing happens to be doing at the time.

2) Executing a Timer Object Function Multiple Times

The timer object supports three multiple execution modes [9]:

- Fixed Rate;
- Fixed Delay;
- Fixed Spacing.

In many ways, these execution modes operate the same:

- The Tasks to Execute property specifies the number of times executions of the timer object function (TimerFcn).
- The Period property specifies the amount of time between executions of the timer object function.
- The Busy Mode property specifies how the timer object handles queuing of the timer object function when the previous execution of the function has not completed.

The execution modes differ only in where they start measuring the time period between executions. Figure 4 illustrates the difference between these modes. Note that the amount of time between executions (specified by the Period property) remains the same. Only the point at which execution begins is different [10].

3) Handling Function Queuing Conflicts

At busy times, in multiple execution scenarios, the timer may need to add the timer object function (TimerFcn) to the execution queue before the previously queued execution of the function has completed. The timer object handles this scenario by using the Busy Mode property. If the value of the Busy Mode property specifies 'drop', the timer object skips the execution of the timer function if the previously scheduled function has not already completed. If specify 'queue', the timer object waits until the currently executing function finishes before queuing the next execution of the timer object function. If the Busy Mode property is set to 'error', the timer object stops and executes the timer object error function (ErrorFcn), if one is specified [10].

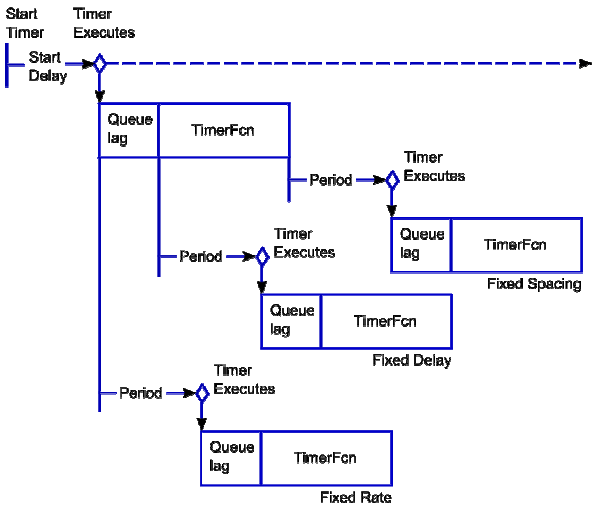

Fig. 4. Differences between Execution Modes

V. Simulation Results

Typical case study is studied in this section, the effect of the Timer Object that scheduling the execution of set of the queries that were shown on real queries. All experiments were done on a 2.40 GHz Pentium Processor with 256 K.B cache memory, 256 MB of memory, and one Disk drive 80 GB. The Operating System which was used is Microsoft Windows XP professional version 2002. The simulation results are executed based on database Microsoft Access2000 is "Northwind.mdb", which contains seven tables. The programming tasks was built by MATLAB version 6.5. The following steps are executed to implement the proposed systems:

- Specify a set of the simple queries inside the file, every query select primary key (numeric field) from all tables in database to efficiently collect information about the database quickly, and accurately at runtime.
- A Timer Object is built for using to schedule the execution the file (previous point). When the timer object fires (multiple times) executes this file, the amount of time specify between executions of the timer object perform the execution of the real queries.
- Real queries are built to test as Q1, Q2, Q3, Q4, Q5, Q6, Q7, and Q8. These queries are varying in join the tables.

A. Simulation Experimental Results

Step1: The first steps, the real queries Q1, Q2, Q3, Q4, Q5, Q6, Q7, and Q8 executed before execution the timer object t and calculated the values execution times of the real queries in variable vector as "Before Execution". The values of the execution times of these queries before execution the timer object t is shown in Fig.5.

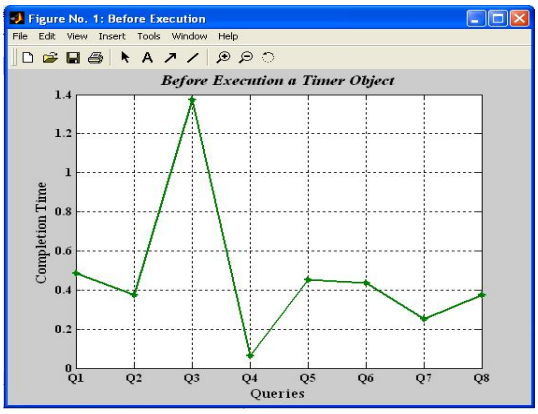

Fig. 5. Completion times of the real queries before execution the Timer Object t

Step2: The Timer Object was built with the set values of the timer object properties that were specify. It was executed the file which contains a set of simple predefined queries in predefined time scheduling to collect estimates of statistics at runtime. When the amount of the time specified by the timer object t elapses (such as 5 secs) and the timer object fires (such as 5 times) executes this file, The amount of time specify (such as 60 secs) between executions of the timer object t perform the execution of the real queries.

Victim times are executed times of the file (simple predefined queries) of every once to collect statistics about database environment in Fig.6 shows these values, calculated the average victim time for all the multiple times executed the file in Fig.7 presents this value, and calculated total victim times when done the work the Fig.8 presents this value.

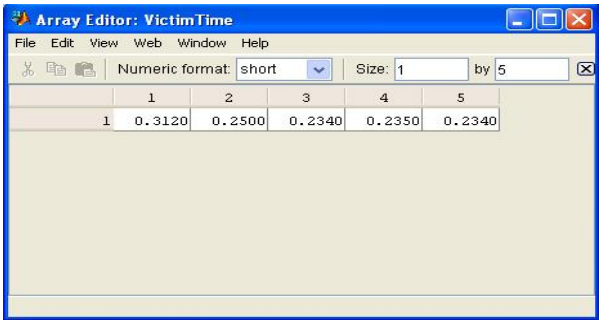

Fig. 6. Execution times a set of simple predefined queries of every once

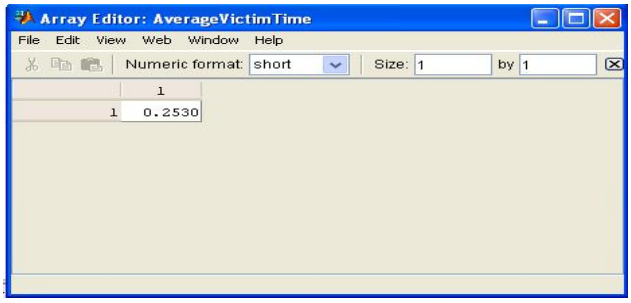

Fig. 7. Average execution time a set of simple queries

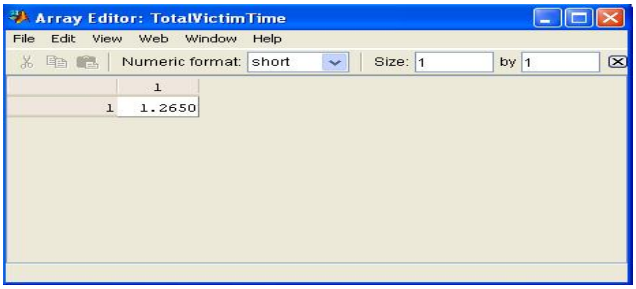

Fig. 8. Total execution times a set of simple queries.

In terminal the work of the Timer Object t (when done the work) has a list of properties that were specified previously whenever a Timer Object t built. A list of all properties of the Timer Object t after the running off is viewed in Fig. 9.

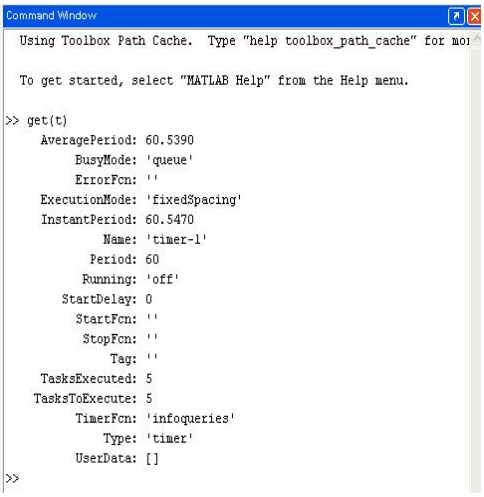

Fig 9. A ist of all properties of the Timer Object t

Step3: Repeat execution the same of the real queries Q1, Q2, Q3, Q4, Q5, Q6, Q7,and Q8 there was executed in step1 after fire execution the Timer Object t and calculated the values execution times of the real queries in variable vector as "After Execution". The values of the execution times of these queries after fire execution the Timer Object t is shown in Fig.10.

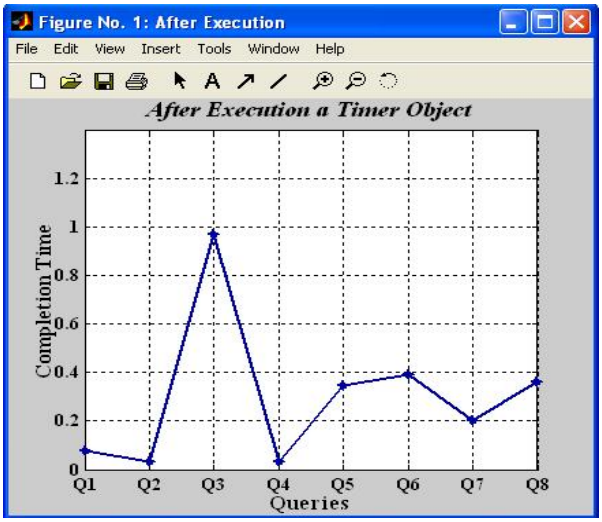

Fig. 10. Completion times of the queries after fire execution the Timer Object t

Step4: We calculated the performance of the Timer Object t on the real queries Q1, Q2, Q3, Q4, Q5, Q6, Q7, and Q8:

1. The difference between completion times for ever real queries before and after fire execution the Timer Object t in the variable vector as "Difference".
2. Calculate the total completion time of the real queries before execution the Timer Object t in the variable vector as "Total Before Execution".
3. Calculate the total completion time of the real queries after fire execution the Timer Object t in the variable vector as "Total After Execution".
4. Calculate the total difference between total completion time of the real queries before and after execution the Timer Object t in the variable vector as "Total Difference".
5. Calculate the improvement in execution real queries in the variable vector as "Percentage Improvement".
6. Calculate the gain time in the variable vector as "Gain Time" from using a Timer Object t.
7. Calculate the percentage gain time for every victim time in the variable vector as "Percentage Gain Time" from using a Timer Object t.

Fig.11 gives the differences between the values of the execution times of the real queries *Q1, Q2, Q3, Q4, Q5, Q6, Q7,* and *Q8* before execution the *Timer Object* ***t*** and the values of the execution times of the same real queries after fire execution the *Timer Object* ***t***.

Also Fig.12 presents the significant improvements on the performance of the real query from using a *Timer Object* ***t***.

VI. CONCLUSIONS

This paper introduces query optimization based on time scheduling approach which is aimed to reduce query re-optimization plan. This approach executes a set of simple predefined queries in predefined time scheduling to efficiently collect estimates statistics quickly and accurately at runtime. For this purpose, a Timer Object incorporates with adaptive query processing systems is proposed to handle the problems with reactive and proactive reoptimization techniques. When the amount of time specified by the timer object elapses , then the timer object fires executing a set of simple queries that were specify, and the amount of time specify (the period time) between executions of the timer object perform execution of the real queries. During this period time, the system is used any previous query reoptimization techniques (Reactive reoptimization approach) doing query execution plan reoptimization if required and this will be very little. Finally, simulation results demonstrated that there are significant improvements on the performance of the real queries due to the time scheduling process.

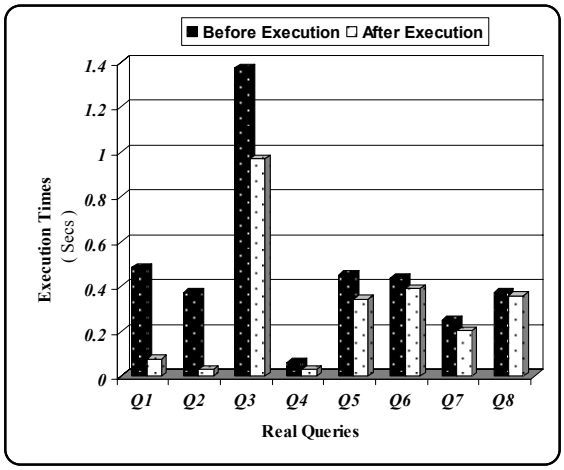

Fig. 11. Execution times of the real queries before and after execution the Timer Object *t*

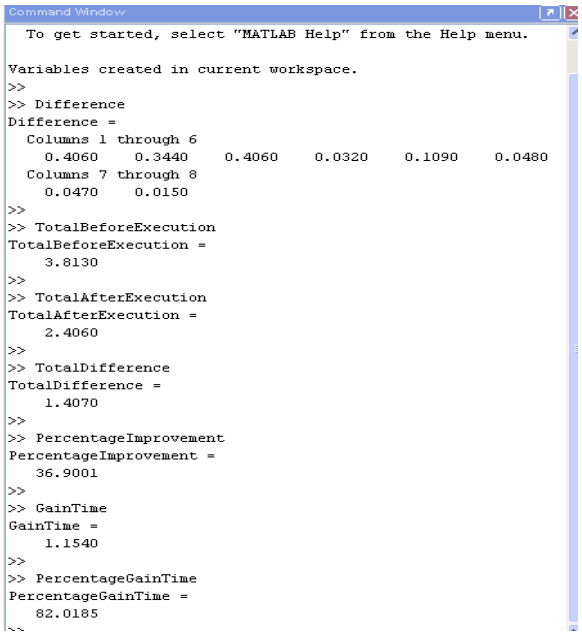

Fig. 12. Improvements on the real queries *Q1, Q2, Q3, Q4, Q5, Q6, Q7,* and *Q8* from use a Timer Object *t*

ACKNOWLEDGEMENT

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A Programmable Built-in Self-diagnosis Methodology with Macro and Micro Codes for Embedded SRAMs

P. Manikandan, Bjørn B. Larsen, Einar J. Aas , M. Areef

Abstract – **Memories are one of the most universal cores that are embedded into almost all system on chips (SoCs). Finding cost effective test solution for embedded memories is paramount. Industries are still improving the existing low cost memory test solutions which can support current technologies and advanced SoC architectures. This paper presents a programmable built-in self-diagnosis (PBISD) methodology with self-test for embedded SRAMs. The BISD logic adapts the test controller with micro code encoding technique in order to control test operation sequences for fault detection. It also encompasses a diagnosis array in order to locate fault sites. The macro codes are used to select any of seven MARCH algorithms, and detect different faults of the memory under test (MUT). This BISD supports the test, diagnosis and normal operation modes. The experimental results show that this work gives 17-47% improved area overhead and 16-41% enhanced speed compared to three published results.**

Index Terms – **Micro code, Macro code, Self-Test, Diagnosis, Memory test.**

I. Introduction

Testing of embedded memories receive growing attention in both industrial and academic researches. Built-in self-test (BIST) of memories is considered as the best solution because of its at-speed test support, on-chip test pattern generation and on-chip response analysis. BIST can also support on-line and off-line tests. On-line BIST has shorter test time but results in area overhead. Off-line BIST employs longer test time but small area overhead. However, area overhead and performance penalty represent two major concerns for SoC testing. Improvements in these measures are extremely important in order to attain high quality testing. Also, the diagnosis of embedded memories is receiving a growing attention in industries [1] while targeting the effective fault analysis, reduced test cost and improved design verification. This diagnosis function is important to reduce the defects per million (DPM) level as well as to help the SRAM design and process engineers to improve the yield during the development stage. Therefore it is desirable to have the combination of BIST and self-diagnosis, such as Built-in self-diagnosis (BISD). This method is the most acceptable solution while locating fault sites of the embedded SRAMs [2-6].

This work combines BIST with a diagnosis array in order to detect the defective memory and its fault location address. It also addresses the improvement of area overhead and performance measures by employing an efficient test controller. This BISD exploits the same macro codes [7-9] for selecting the test algorithm. [7] introduced structured programmable memory BIST (PMBIST) with online programmable capability using "macro command". In which, the memory BIST (MBIST) controller unit is used to produce the correct sequence of MARCH elements according to the selected test algorithm. In [8], PMBIST employs FSM based algorithm generator and test controller which are used to control MARCH elements and test data. The PMBISTs of [7] and [8] provides simplified macro command based test methods in order to achieve flexibility feature, reduced test time and test data. However, there is an area overhead due to their state machines dependability on certain conditions like last memory address run on the MARCH element and the additional sequence counter. The similar PMBIST approach was stated in [9]. It used the same encoding technique for the MARCH elements but instead of using state machines as in [7] and [8] the test controller was designed using clusters of microcode which controls the read/write operation and test data injection. Also it requires less number of states to perform read and write operations. Thus, an improved performance of the test controller and minimizing the area overhead can be achieved if an efficient coding technique is employed especially in read/write operation FSM. This paper used an efficient encoding technique with dual operation segments (OS1 and OS2) while assigning micro codes to MARCH elements.

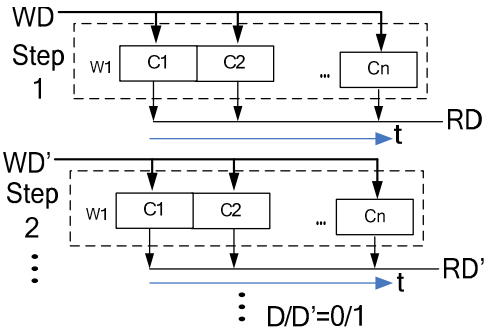

Fig. 1. Basic memory test with write/read operation

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Generally, memories are used to store (write operation) and retrieve the data (read operation) by addressing specific memory locations. This basic concept is also used in memory testing as shown in Figure 1. In memory testing, according to the algorithm and fault model there will be consecutive write and read operations of test patterns (0/1) with respect to time. The correct output response will be expected from each memory cell during the read operation. If the actual output is different from the expected output then it is considered that the memory has defect. MARCH based test techniques are most commonly used in memory test because it is simple and provides good fault coverage [10-16]. It supports a sequence of read or write operations that examines the memory either in ascending or descending address order.

Table I.
FAULT DETECTION OF MARCH ALGORITHMS

Test Algorithm	Description	Fault detection		
		SAF	TF	CF
MATS+	{⇑⇓ (w0); ⇑ (r0, w1); ⇓ (r1, w0)}	Yes	No	No
MARCH X	{⇑⇓ (w0); ⇑ (r0, w1); ⇓ (r1, w0); ⇑⇓ (r0)}	Yes	Yes	Yes
MARCH A	{⇑⇓ (w0); ⇑ (r0, w1, w0, w1); ⇑ (r1, w0, w1); ⇓ (r1, w0, w1, w0); ⇓ (r0, w1, w0)}	Yes	Yes	Yes
MARCH B	{⇑⇓ (w0); ⇑ (r0, w1, r1, w0, r0, w1); ⇑ (r1, w0, w1); ⇓ (r1, w0, w1, w0); ⇓ (r0, w1, w0)}	Yes	Yes	Yes
MARCH C-	{⇑⇓ (w0); ⇑ (r0, w1); ⇑ (r1, w0); ⇓ (r0, w1); ⇓ (r1, w0); ⇑⇓ (r0)}	Yes	Yes	Yes
MARCH U	{⇑⇓ (w0); ⇑ (r0, w1, r1, w0); ⇑ (r0, w1), ⇑ (r1, w0, r0, w1), ⇑⇓ (r0)}	Yes	Yes	Yes
MARCH LR	{⇑⇓ (w0); ⇑ (r0, w1); ⇑ (r1, w0, r0, w1); ⇑ (r1, w0); ⇑ (r0, w1, r1, w0); ⇑⇓ (r0)}	Yes	Yes	Yes

SAF - Stuck-At Fault, TF – Transition Fault, CF – Coupling Fault

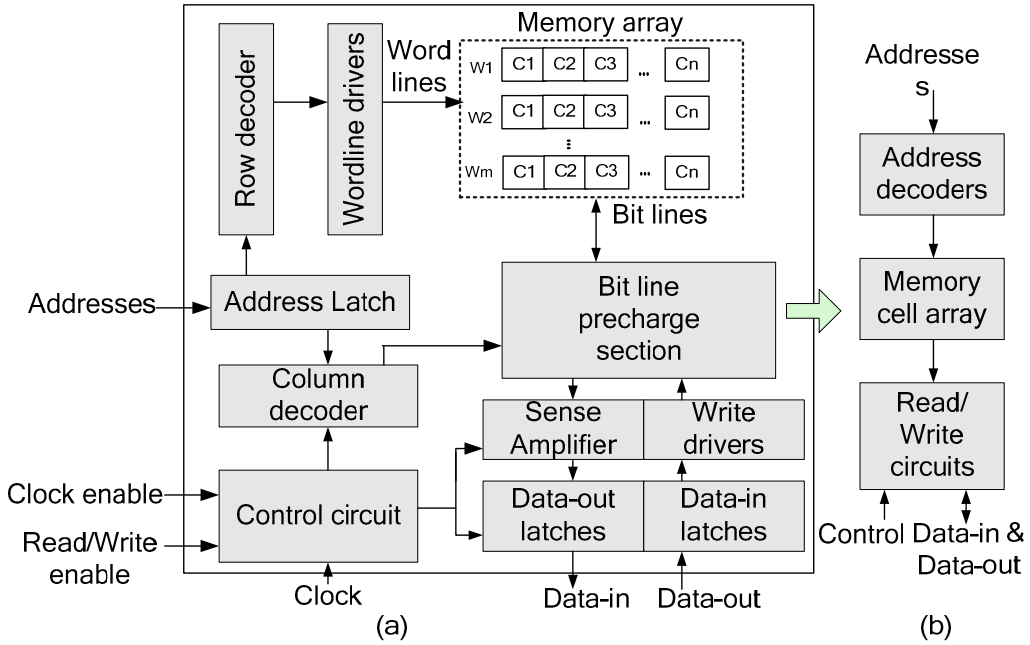

Fig. 2. Functional model of RAM chip (a) and reduced functional model (b) [14]

Some of the MARCH based algorithms and their descriptions with fault detection are presented in Table 1, using Van de Goor [14] notation. Refer to Section 2.1, for fault definitions. In Table 1, (i) w0 and w1 represents writing 0 and 1 into a cell, (ii) r0 and r1 represents reading 0 and 1 from a cell, respectively. ⇑ and ⇓ denotes memory address order increment and decrement, respectively. ⇑⇓ denotes either memory address order increment or decrement and the description shows the algorithm steps. Generally, MARCH based test algorithms supports a sequence of read or write operations that examines the memory either in ascending or descending memory address order. For example in MARCH C- algorithm with m words × n bits memory under test, the algorithm begins writing 0s from location 0×0 with ascending address order increment. The write operation continues until it reaches the last bit of the memory array or m×n. Then it reads 0s from the memory array in ascending order and checks whether the same data (0s) is available or not. Next, it changes the content of every cell by 1 and then reads back the same data in ascending order. This read operation expects 1s from every cell of the memory array. Again the write operation writes 0s into all memory cells in ascending order. Similarly, the same test operation repeats in descending order as shown in the description of MARCH C- algorithm in Table I. In this paper we consider Static RAM with flexible test features. This programmable memory BISD (PMBISD) technique supports seven MARCH test algorithms, and the number was chosen in order to make a

fair comparison with existing works [7-8]. The algorithms were chosen based on their effectiveness, fault coverage and industry test results analysis [17].

The rest of the paper is organized as follows. Section II shows the overview of memory and its fault distribution with summary of different test algorithm types. Section III introduces the architecture of PMBISD with macro and micro codes. Section IV describes the details of the functional flow and diagnosis array. Section V illustrates the experimental results. Section VI concludes this work. Finally, Section VII gives discussions and future directions.

II. Overview of MBIST

Figure 2(a) shows the general model of an SRAM chip. The simplified functional model of the SRAM chip is also given in Figure 2(b) [14], including the control line which provides the clock signal to control the timing behavior of read/write operations. As indicated in Figure 2(a), the address latch contains the current address. The higher order bits of address are connected to the row decoder which is used to select a row and the lower order address bits are connected to the column decoder which is used to select the required columns in the memory array. In the memory array, several adjacent memory cells are connected to form a single word line. The number of adjacent cells depends on the data width of the chip since each cell corresponds to a single bit operation. Several word lines are connected to form a memory array. During the write operation, the write enable signal is active and therefore the data is written into memory through the write drivers and bit lines. Similarly, during the read operation the read enable signal is active. Here the data of the selected cells can be read from the memory through sense amplifiers. The data-in and data-out lines are used to transfer the data between memory and external world. These lines are bidirectional, thus reducing the number of pins of the chip. The testing target is to detect the occurrence of different faults in the memory array or peripheral circuits. The possible faults and their distribution among the memory chip are discussed in the next subsection.

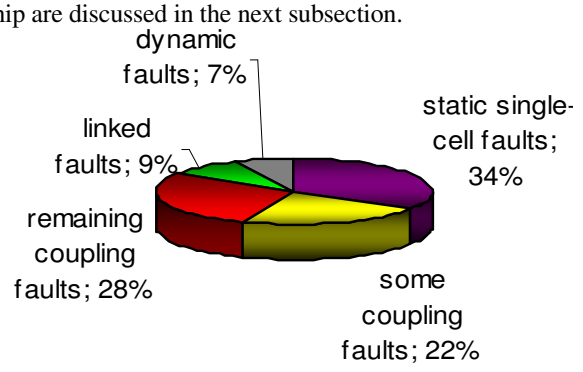

Fig. 3. Memory Faults Distribution [17]

2.1 *Fault Distribution*

The functional faults of memory can be classified into four categories [14]. In the first category, faults involving only in a single cell are placed. For example (i) Single-cell stuck-at fault (SAF) – the cell contains 0 instead of 1 (SA0) or 1 instead of 0 (SA1), and it remains at the same value. (ii) Transition fault (TF) – the cell cannot go through 0 to 1 or 1 to 0 transitions. In the second category, there are faults in which two cells are involved. For example, coupling faults (CF) – the victim (coupled cell) is forced to 0 or 1 when the aggressor (coupling cell) updates its values to 0 or 1. In the third category, there are faults in which k cells are involved. For example the k-coupling, the bridging and the state coupling faults. The bridging and state coupling faults are special cases of the general coupling fault model. Fourth, and the last category is accommodating faults that are the neighborhood pattern sensitive faults. In addition to the faults mentioned in [14] and Table I, there are also some other complex fault models like linked faults (LF) [20] and dynamic faults (DF) [21] considered by researchers. Faults requiring more than one operation sequentially in order to be sensitized are called dynamic faults and linked faults are faults that influence the behavior of each other. M. Linder et al [17] analyzed and summarized the distribution of complex memory faults in addition with basic faults along the chip. The data from [17] is shown here to give an idea to readers about different types of faults distribution along the chip (Figure 3) and the fault coverage values of different MARCH like algorithms (Figure 4) based on the industry test results and its credits will go to corresponding authors. In Figure 3, the amount of all coupling faults is about 50%. It includes some coupling faults – 22% detected by type II, and remaining coupling faults – 28% detected by type III algorithms of Table II. Then the basic single cell faults are 34% and complex memory faults (LF and DF) results 16% in the total faults distribution. These complex faults can be only detected by some specific algorithms such as MARCH AB, MARCH LR and MARCH LA.

2.2 *Fault Detecting Algorithms*

Functional test algorithms are targeting defects between memory cells, or within a single memory cell by applying test patterns, and performing output response analysis. These test algorithms basically write 1s or 0s into all memory cells in order to detect individual cell defects. As shown in Section 1, MARCH-like algorithms begin by writing a background of zeros. Then it reads the data at the first location and writes a 1 to that address. It continues the read/write procedure consecutively until the last address is reached. The test is then repeated for different read/write sequences according to the algorithm. The test length is of order N, where N is the number of words in the memory [18]. These algorithms can find cell opens; shorts; address uniqueness; and some cell interactions. Some early algorithms considered faults only related to simple static type [14], [19], whereas a few recent algorithms are covering other and complex faults like linked or dynamic faults [20], [21]. [17] groups the algorithms into five types/sets as shown in Table II. It also demonstrates the effectiveness of different memory test algorithms based on a comprehensive analysis of empirical test results as given in Figure 4. This analysis helps to optimize the selection of memory test algorithms with respect to their efficiency. An effective selection of test

algorithms leads to high quality test with low test time. However, this work considered only few efficient MARCH based algorithms from Figure 4. The chosen algorithms are mainly from Type II, III and IV of Table II as given in Table I. The reader may refer to the source for analyses of different memory test algorithms.

III. Architecture of PMBISD

The I/O port model of the PMBISD is shown in Figure 5. This BISD scheme can support seven test algorithms as shown in Table 1 which includes the basic test algorithms (MATS+, MARCH X, MARCH A, MARCH B, MARCH C-) plus the advanced memory test algorithms (MARCH U and MARCH LR). This number of algorithms was considered in order to make a fair comparison with earlier programmable BIST with macro codes. 3-bit Macro codes (MaC) 000, 001, 010….110 are assigned to the algorithms MATS+, MARCH X …. MARCH LR, respectively. In this model, test_h is used to select either operation mode such as normal operation (NO) or test operation (TO). Similarly, test_d is used to enable diagnosis operation of the BISD circuit. The hold signal is used to stop the BIST operation during the test mode and keep the current data / address when required. Clk is the memory BISD clock signal. During the BIST operation, if any memory defect is detected then fail_h goes high. At the completion of the BIST operation, tst_done signal goes from low to high and the diagnosis operation results in the faulty address and data through scan_out, AO_mem and DO_mem.

Table II.
Fault Detection Capability of Different Algorithms

Type	Source	Algorithms	Detecting Faults			
			SS	CF	LF	DF
I	[14], [19]	Scan, Scan+	Yes	-	-	-
II	[14], [18], [22]	MATS, MATS+, MATS++, MARCH X, MARCH C-, MARCH Y, PMOVI, MARCH 1/0, MARCH TP, MARCH C+, MARCH A, MARCH B and MARCH SS	Yes	Yes	-	-
III	[23], [24], [25]	Algorithm B, MARCH U, MARCH SR	Yes	Yes	-	-
IV	[26], [27]	MARCH LA, MARCH LR	Yes	Yes	Yes	-
V	[21], [28], [29], [30], [31]	MARCH RAW, MARCH AB, MARCH BDN, Hammer 5R, MARCH G	Yes	Yes	Yes	Yes

SS – Static Single-cell Fault, CF – Coupling Fault, LF - Linked Fault, DF – Dynamic Fault

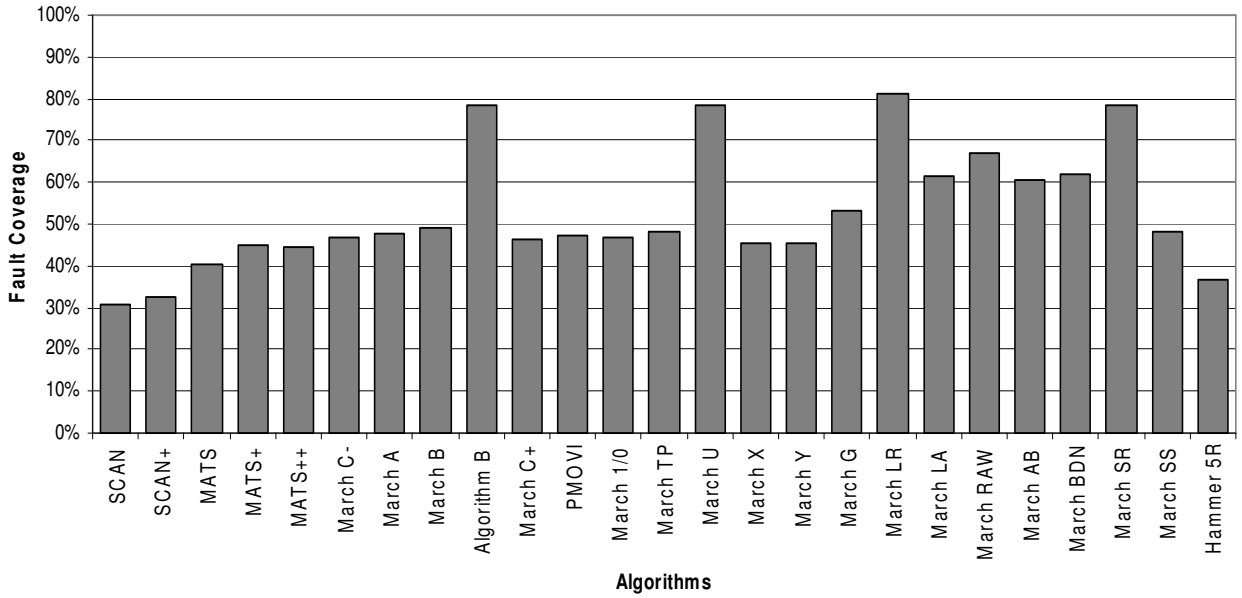

Fig. 4. Effectiveness of Memory Test Algorithms [17]

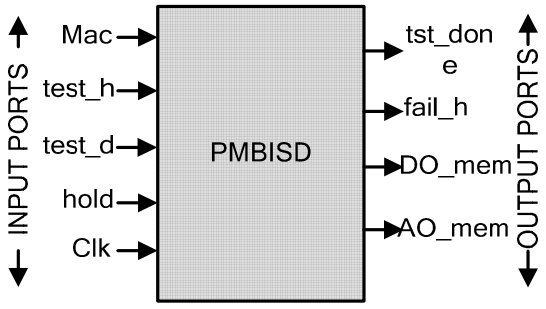

Fig. 5. I/O Port Model of PMBISD

A simplified architecture of PBISD is given in Figure 6 with their internal signal flow. The internal signal descriptions are given in Table III. The memory to be tested is showed in the shaded background. The test circuitry is composed of an algorithm selector, address decoder, test controller, test pattern generator and diagnosis array. The test set-up also consists of the comparator in order to evaluate the acquired data of MUT.

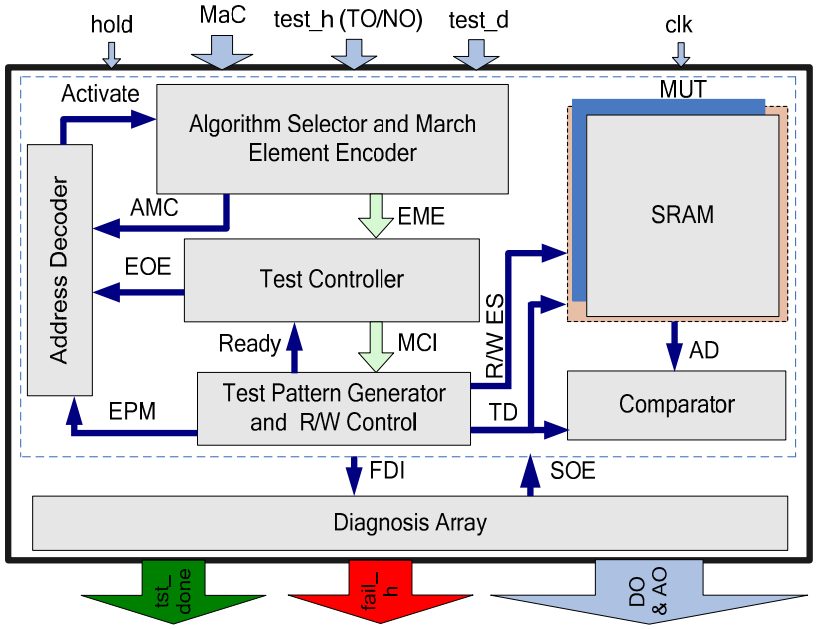

Fig. 6. Architecture of BISD

3.1 Algorithm Selector and Test Controller

This BIST design can be programmed on-line using Macro commands in which the algorithm selector is used to select the test algorithm through 3-bit macro codes. Each MARCH algorithm has a sequence of MARCH elements (ME) which can be encoded into 4 bits micro opcode as shown in Figure 7. It uses 11 MEs to represent seven algorithms. The given opcode in Figure 7 is not including the address direction bit. Algorithm selector gives the encoded MARCH elements (EME) of the selected algorithm to the test controller as well as the address sequence micro code (AMC) signal to the address decoder. The test controller is using two operation segments (OS1 and OS2) while assigning micro codes to the MARCH elements. Each MARCH element has different number of operation sequences and they can be encoded into OS1 and OS2. According to the algorithm execution the MARCH elements are encoded into either single operation or double operation segments. Then the corresponding micro code instructions (MCI) through the test pattern generator are used to control read/write operation sequences.

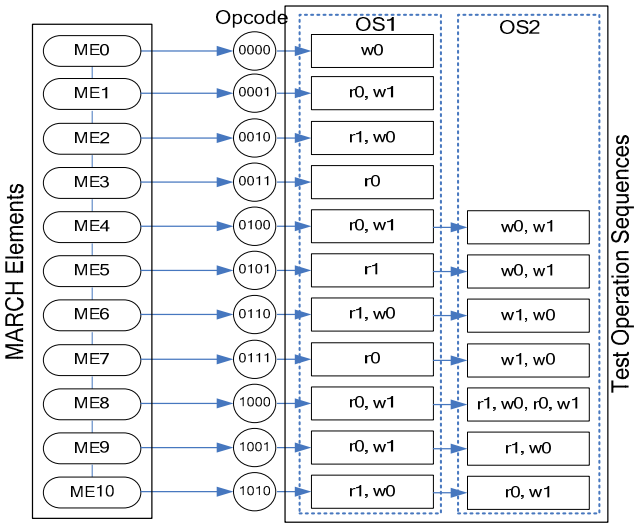

Fig. 7. Micro op-codes with MARCH Elements and Operation Segments

While implementing ME8 this work results r0, w1 into OS1 and r1, w0, r0, w1 into OS2. There are 4 operations in a single segment (OS2). For this same problem, [9] encoded ME8 into triple clusters (Cluster 1, Cluster 2 and Cluster 3). Each cluster can support single or double read/write operations. For instance, each cluster is encoded into three individual MARCH elements 9, 11 and 12. Again, MARCH element 9 has two dual operation clusters and each element of 11 and 12 has two dual operation clusters and one single operation cluster. The method in [9] needs micro code instructions to control 14 read/write operations. But this work used only double operation segments in order to increase the speed while assigning micro codes to the respective MARCH elements. We programmed to encode OS2 of ME8 into 1010 without affecting the operation sequences of test algorithms. It needs three operation segments and its corresponding micro code instructions are used to control only 6 read/write operations. When the test controller completes the encoding process, it gives the end of operation encoding (EOE) signal to the address decoder. The address decoder gives Activate signal to the algorithm selector in order to indicate that the test controller is ready to receive the next MARCH element.

Table III.
INTERNAL SIGNALS DESCRIPTION

Internal Signals	Description
EME	Encoded MARCH Element
AME	Address Micro Code
EOE	End of Encoding Operation
MCI	Micro Code Instructions
EPM	End of the process of MCI
R\W ES	Read/Write Enable Signals
TO	Test Operation
NO	Normal Operation
TD	Test Data
AD	Acquired Data
A&D	Address & Data
FDI	Fault Detection Information
SOE	Scan out Enable

3.2 Test Pattern Generator and R/W Control

During the BIST operation, the test controller is used to control read/write operations in MUT. It provides micro code instructions (MCI) to the test pattern generator in order to control the test data sequences and address order increment/decrement. Then the test pattern generator decodes these MCIs and gives read/write enable (R/W ES) signals and test data (TD) to the MUT with operation sequences. When the operation reaches the last address and at the end of read/write operation encoding, the test pattern generator gives end of the process of micro code instructions (EPM) to the address decoder and also ready signal to the test controller. The increment/decrement of the addressing order is achieved by a direction bit together with appropriate micro code.

In test mode, the generated test data (TD) by the test circuitry is applied to the SRAM, and according to the test algorithm MUT will be examined by the corresponding operation sequences. The acquired data (AD) of MUT will be compared with the actual data in a comparator. If the comparison results in mismatch, then it indicates a defective memory. Then the signal fail_h goes high. Fault detection information (FDI) and scan-out enable (SOE) signals are bridging the built-in self-test controller and diagnosis array. In diagnosis mode, the scan_out signal gives the faulty memory address (AO_mem) and the faulty memory data (DO_mem) at the output. The functional flow with diagnosis operation is described in the next section. However, the test controller of this BISD provides less area overhead due to the absence of the sequence counter. It also provides improved speed due to its double operation segments with efficient reuse of MARCH elements. As well as this micro code encoding technique is not depending on the last address insertion.

IV. FUNCTIONAL FLOW AND ANALYSIS

The input ports, test_h and test_d are used to select the functional mode of the BISD. This BISD scheme supports four different modes such as normal operation, BIST/test operation, diagnosis operation and hold operation. The functional flow of the BISD is illustrated in Figure 8.

4.1 Functional Flow Chart

As shown in Figure 8, the operation begins by asserting test_h signal to either low or high. When test_h=0, it starts the normal operation (mode 1) and test_h=1 enable the BIST operation (mode 2). If there is fault detection then fail_h signal goes high and at the end of the BIST operation tst_done signals goes high. However, by asserting test_d signal to high the diagnosis operation (mode 3) starts. Diagnosis operation mode enables the shifting out of address and data signals of the failed location of the memory. The scan_out signal is active in this mode and it scan out the faulty address and data from memory. The BIST operation continues the testing process while the active test_d signal scan out the faulty site data. During BIST and diagnosis operations hold signal keeps logic 1. If we assign logic 0 to hold signal, it stops the operation and hold the current address and data.

Diagnosis

Diagnosis operation is used to identify the faulty site of the MUT. For this purpose the test circuit adapts the diagnosis array with shift counter and diagnosis fields as shown in Figure 9. The three diagnosis fields (DFs) are corresponding to the faulty address (FA), faulty data (FD) and faulty pulses (FP). When test_d signal is active the diagnosis array receives fault detection information (FDI) from the test circuit. Then the diagnosis array gives scan out enable (SOE) to the BIST circuit and activates the scan_out signal. When a faulty word is detected in MUT, it transfers the corresponding faulty address and data to the output ports (AO_mem and DO_mem) through DFs of the diagnosis array. This BISD also gives faulty pulses through fail_h signal. This BISD circuit continues the testing while shifting the faulty address and data. After completing the test process in all addresses of the MUT according to the algorithm the tst_done signal goes high. It indicates the end of the BISD operation.

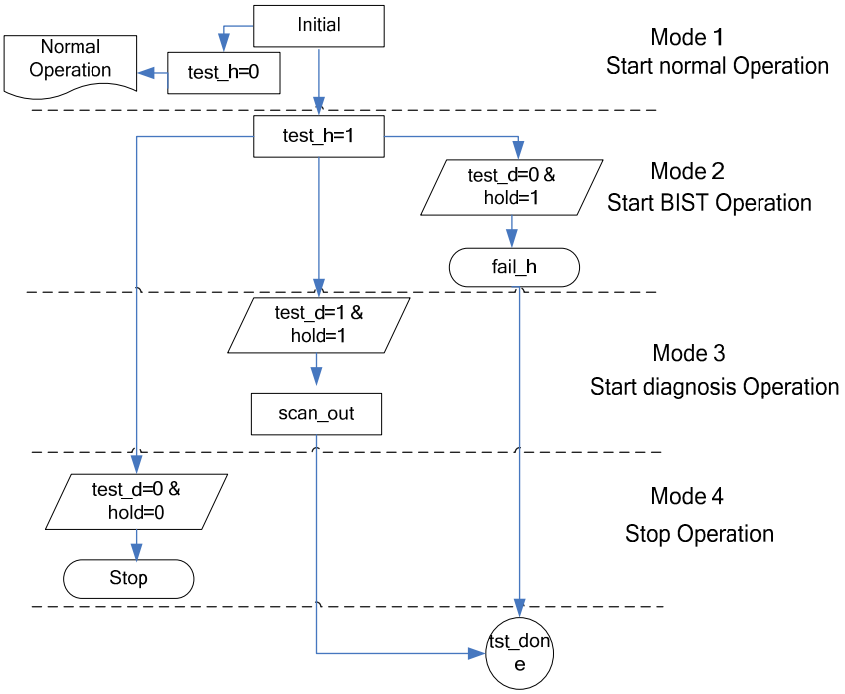

Fig. 8. Functional flow of BISD

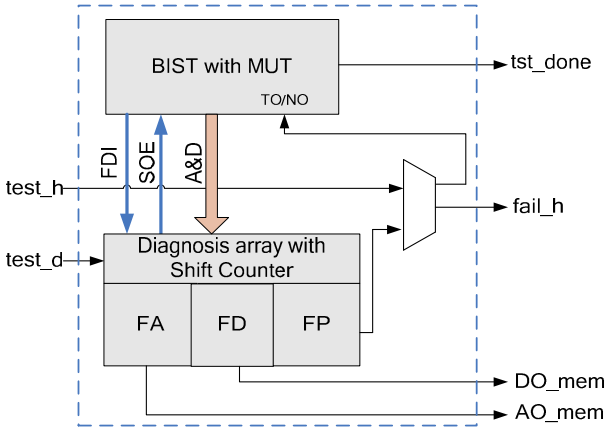

Fig. 9. Diagnosis Operation

The previous PMBIST [7] [8] consists of the sequence counter in the test controller in order to control the read/write operations. Even though our test controller avoids the sequence counter because of an efficient encoding technique of MARCH elements, the shift counter and DFs of the diagnosis array costs additional area overhead. However, the performance and area overhead of our test controller is better than existing PMBISTs and the comparison results are given in the next section. The faulty data output of the BISD helps design engineers to locate the faulty site in a memory array and improve the SRAM design in the early phase of the circuit design. The obtained faulty data can be represented in the form of MARCH signatures in order to analyze the fault location. For example, a MARCH test detects a faulty cell during the read operations. Also the read out data is available in the output port. If we make the MARCH signature of the consecutive read operations of a memory cell, it helps to analyze the type of fault with fault site. Let us consider a single cell in a word and expect a MARCH signature (correct data) of that particular cell as 01010. After completing the test process if the MARCH signature is 00000 then it concludes the cell failure occurs during the second and fourth read operations. Even though this signature comparison helps to locate the faulty cell in a word, when we consider the large size memory it is reasonable to label the read operations of MARCH tests with fault dictionary. For each fault model we can compare the signature of every faulty cell. Since the fault analysis is not the focus of this paper, the reader may refer more about the concept of fault dictionary, MARCH signatures and memory fault simulator in [32].

IV. Experimental Results

This section shows the experimental results of a programmable MBIST with macro and micro code encoding techniques for a synchronous single port SRAM. In order to show the functional verification of our work, case simulations had been done and results are shown in Figures 10 (a), (b) and (c). In order to have a fair comparison with existing work, Mentor Graphic's Precision tool has been used to synthesize the test circuit. The results are compared with the previous programmable MBIST test controllers.

Case 1: Fault Free Simulation

Figure 10 shows the simulation waveform of the fault-free SRAM. In which, the BIST mode was enabled by high test_h signal and it also has high hold_l signal. The

comparator gives match result for fault-free memories and therefore fail_h signal is in logic low status. After completing the BIST operation, tst_done signal goes high, indicating the end of the test mode.

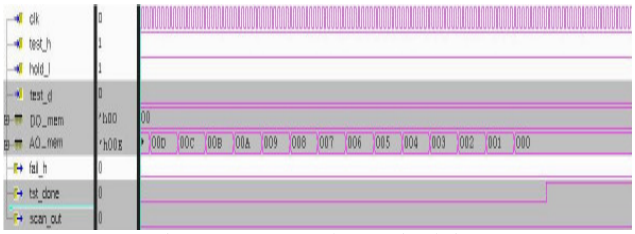

Fig. 10. Case 1 – Fault Free Simulation

Case 2: Fault Simulation

Figure 11 shows the simulation waveform of the faulty SRAM. In this case simulation, MARCH C- algorithm was executed. The SRAM model is also modified to be in defective state by inserting single-cell faults. The BIST mode was enabled by high test_h signal and also it has high hold_l signal. The comparator gives mismatch result in the faulty locations. Therefore the fault detect waveform fail_h gives high pulses when faults are detected.

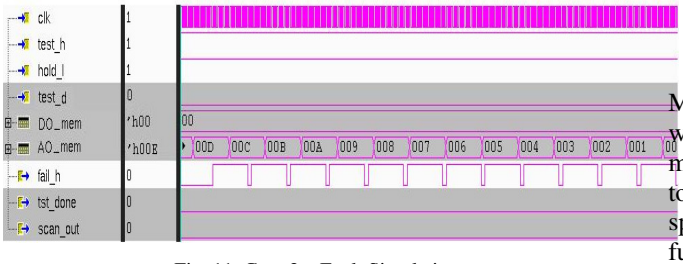

Fig. 11. Case 2 – Fault Simulation

Case 3: Diagnosis Operation

Figure 12 shows the simulation waveform of the diagnosis operation. In this case, test_d signal is high. When the BIST operation finds defect, its corresponding fault data and faulty address are shifted to the output ports DO_mem and AO_mem, respectively. The fault pulses are indicated by fail_h signal.

AREA OVERHEAD AND SPEED COMPARISON

Source	Area Overhead		Speed (MHz)	
	6A	7A	6A	7A
[7]	74LE	-	116.58	-
[8]	-	81LE	-	82.17
[9]	49LE	52LE	125.38	118.27
This work	40LE	43LE	149.32	140.24

Fig. 12. Case 3 – Diagnosis Operation

Synthesized Results

This PMBIST was synthesized for two different number of test algorithms such as six (6A) and seven algorithms (7A) with adapted test controller. Noor [9] synthesized PMBIST test controllers and showed the test results in terms of logic elements (LE). For the comparison, the synthesized results of our BIST controller in terms of logic elements (LE) are shown in Table IV. First, the test setup with 6A achieved improved area overhead and speed which are 18-46% and 16-22%, respectively. Similarly, the second case (7A) gives 17-47% improved area overhead and 16-41% improved speed than previous works. Also the time results for BISD that implements all the six and seven test algorithms are 9.11ns and 10.86ns, respectively. This proves that the proposed approach reduces the number of required cycles and it results less execution time than [7] and [8]. In this method, micro-code needed to execute the selected test algorithm is considerably reduced while controlling the test operation sequences. The dual segments technique efficiently utilizes the available MEs. However, when we include more algorithms the complexity of the test controller as well as the number of MARCH elements and its storage requirements will increase. It may result in more area overhead while sacrificing the speed.

V. CONCLUSION

In this paper, the programmable BISD architecture and its MARCH test algorithms with operation segment technique were presented. The experimental results show that this method results in 17-47% improved area overhead compared to [7], [8] and [9]. It also has the advantages of improved speed, and simple to control test procedure. The diagnosis function is used to identify the faulty location by reading faulty address and faulty data from MUT. This will help the SRAM design and process engineers to improve the circuit and yield during the development stage. However, an efficient reuse of existing MARCH elements will help to add or replace less complex MARCH test algorithms, without the need to redesign the entire circuitry.

VI. DISCUSSIONS AND FUTURE DIRECTIONS

The flexibility feature of our BISD allows adding more MARCH algorithms with the cost of additional area overhead and performance degradation in the test controller. The cost depends upon the complexity of the newly added algorithm. For example from Table I, let us consider MARCH U and MARCH LR algorithms with the test length of 14n. If either or both algorithms are replaced by MARCH G and/or MARCH RAW with the test length of 23n+2D and 26n respectively, then the complexity of implementing test sequences will also increase. According to the description of MARCH RAW algorithm it requires the test sequences for ⇑(r1,w1,r1,r1,w0,r0);⇓(r0,w0,r0,r0,w1,r1);⇓(r1,w1,r1,r1,w0, r0). Even though dual segments technique can handle six operations in each ME as shown in ME8, in order to implement this algorithm in the current architecture, the required number of MARCH elements will be increased. This will automatically increase the area overhead and influence the performance of the test controller. In this

current work, we have chosen the selective algorithms based on two factors which are their efficiency in terms of fault coverage and sequences of MEs where it can be shared efficiently. Therefore, this architecture cannot be applied universally but it is possible to utilize this structure with additional cost. Thus, the existing works differ in a way of using the number of MARCH algorithms and its corresponding MEs, implementation of the test sequences control and micro code encoding technique with improved measures [2-9].

However, when we consider the future directions, it is interesting to note from Figure 4 that the fault coverage is only based on single algorithms. There is not much work about the analysis of combinations of different memory test algorithms (MARCH-like and MARCH-unlike) in a test set. While testing memories, the combination of different test algorithms gives better fault coverage and yield improvement than using a single algorithm. When we use the combination of different algorithms, each algorithm may detect more number of unique faults. The concept of the union and intersection of the fault coverage is used to determine the efficiency of such an algorithms combination [17]. If we consider two algorithms in the combination, the union is the combined fault coverage of both algorithms and the intersection is the number of unique faults that are detected by both algorithms. This is also a challenging task to determine an efficient combination of algorithms with low intersection.

M. Linder [17] discussed about the efficient algorithms combination based on industry test results. For example, MARCH U and Hammer 5R results low intersection in their fault coverage. It means that the number of faults detected by each algorithm is high, but the number of fault detected twice is low. The implementation of such combinations in BISD/BIST will cover different types of memory faults with high fault coverage. Finding efficient combinations of algorithm pairs and their realizations are still open to research in order to cover more complex fault models like dynamic or linked faults, in addition with detecting traditional faults (Single Cell Faults and Coupling Faults).

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Coverage Problem Solving on Quantum Computing

Hahanova I.V.

Abstract – **The qubit (quantum) structure of data and computing processes that allows significantly increasing the speed of binary optimization problem decisions was proposed. The hardware parallel models (one cycle) for Boolean (set of all subsets) calculation on the basis of n-element universum for coverage decision solutions, boolean function optimizations, compression of data, digital systems synthesis and analysis that use the Hasse diagram for implementation processor structure were described.**

Index Terms – **quantum computing, hardware model, Boolean function, processor.**

I. Introduction

The purpose of the qubit-processor creation is significant reduction of time that needs to decision of the optimization problems by using concurrent calculation of the vector logical operations [1-3] over the set of all subsets of the primitives through the cost of increasing the memory size for intermediate data saving. Problems of the research are the follows: 1) Definition of data structures for boolean decision coverage problem of columns of a matrix $M = \left|M_{ij}\right|, i = \overline{1,m}; j = \overline{1,n}$ by ones from the rows. In particular, for case m = n = 8, It should be done the concurrent boolean operation on 256 combinations of the vectors (the matrix rows) that form boolean. 2) The instruction set processor should have m-bit vector operations: and, or, xor; 3) Developing of the qubit-processor architecture for concurrent processing of the $2^n - 1$ data combinations that direct to the optimal solution of the NP-complete coverage problem; 4) Qubit-processor prototype implementation into PLD and hardware model verification [2-13] based on the boolean function optimization solutions. 5) Bringing other practical discrete optimization problems to a form of the coverage task that allows processing them on the qubit processor. As an example it was solved searching of the minimal row number that cover all 1's in columns of the following matrix M:

M	1	2	3	4	5	6	7	8
a	1	.	.	.	.	1	.	.
b	.	.	1	.	.	.	1	.
c	1	.	.	.	1	.	1	.
d	.	1	.	1	.	.	.	1
e	.	1	.	.	1	.	.	.
f	1	.	1	.	.	1	1	.
g	.	1	.	1	.	.	.	1
h	.	.	1	.	1	.	.	.

The computation complexity of the problem solution depends of checking of all 255 row combinations: one with 8 rows, two with the others, three, four-, five, six, seven, and eight. The optimal solution is the minimal number of rows forming coverage. There can be some optimal solutions. The Hasse diagram is a compromise between time and memory size, or solution strategy where previous results are used to form the next more complex superposition. Therefore, it is necessary for each cover table that consist of n primitives (rows) to create own multiprocessor structure in form of Hasse diagram, that can be used for NP full, problem solution. For example, figure 1 shows the Hasse diagram multiprocessor structure for the four row table.

Optimal solutions coverage problem for the matrix M that generates 255 possible combinations are presented at the form of DNF lines: $C = fgh \vee efg \vee cdf$. Finite state machine for the quantum computing process structure by bottom-up analysis of vertices based on the implementation of the following step sequential:

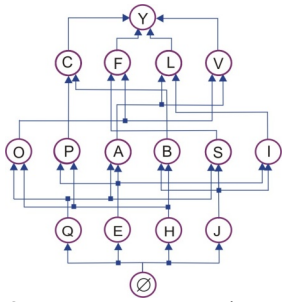

Fig. 1. Quantum structure computing processes

1. Store information in the registers of the primitives (matrix) $L_i^1 = P_i$ of the first level, followed by an analysis of the coverage quality of the each primitive in a binary format (1 - a covered, 0 - no covered). If one of the

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primitives forms the full coverage $\bigwedge_{j=1}^{m} L_{ij}^{1} = 1$ the process of analyzing the Hasse diagram are finished. Otherwise, the transition (r = r + 1) to the next level of the graph are executed:

$$L_i^1 = P_i \to \bigwedge_{j=1}^{m} L_{ij}^1 = \begin{cases} 0 \to n = n + 1; \\ 1 \to \text{end}. \end{cases}$$

2. Initialize the next (second) level of the process. Consistently implement the vector (matrix) operations (or $L_i^r = L_{ij}^{r-1} \bigwedge_{j=1}^{m} L_{tj}^{r-1}$, and $\bigwedge_{j=1}^{m} L_{ij}^{r} = 1$) in order to analyze the coverage ability of the r-level primitive combinations. Here $t = \overline{1,m}$, $i = \overline{1,m}$, $r = \overline{1,n}$, where n is the number of levels or the number of rows in the cover table, m is the number of columns in it. If a combination of at the present level creates a full coverage, which forms an assessment equal to 1, the processing of all subsequent levels of the processor is canceled. Otherwise, the transition to the next level of analysis of the structure of the processor:

$$L_i^r = L_{ij}^{r-1} \bigwedge_{j=1}^{m} L_{tj}^{r-1} \to \bigwedge_{j=1}^{m} L_{ij}^{r} = \begin{cases} 0 \to r = r + 1; \\ 1 \to \text{end}. \end{cases}$$

To find the best coverage is always enough to have only two elements of the lower level. It means that all operating vertices have got two register (matrix input), which significantly reduces the cost of the hardware design. The number of time cycles for processing structure of the processor is equal n in the worst case. You can create an algorithm for finding the optimal coverage through top-down analysis of the vertices. In this case, finding the full coverage in one of the levels needs another structure descending to make sure that there is no bottom to the next level of complete coverage. If it is right the obtained solution is optimal. Otherwise the down levels should be analyzed until the adjacent layer will not contain complete coverage. The vertices of processor structures can have more than one binary (unary) the register logical operation. Then you need to create a simple instruction decoder to enable other operations, for example: and, or, xor, not. Thus, the advantages of Hasse qubit processor (Quantum Hasse Processor - QHP) is the ability to use no more than a 2-input gates for the vector logical operations (and, or, xor), and thus, substantially reduce the cost of implementation by Quine of the processing elements (vertices) and memory through the use of sequential computations and a slight increase in processing time of all vertices of Hasse diagram. For each vertex the quality coverage measure is the presence ones in the all coordinates of the vector result. If the quality criterion is satisfied all the other calculations can be escaped, because the Hasse diagram is a strictly hierarchical structure according to the number of combinations in each levels. This means the best solution is at a lower level of the hierarchy. The same level options are equivalent to implementation, so the first high-quality coverage $(Q = \sum_{i=1}^{n} q_i = n)$ is a better solution that suggests stopping evaluating of all further strategies of the Hasse diagram.

Considering the sequence-concurrent strategy of the vertex analysis of time that is taken to process all primitives of the QH-processor is equal to the number of hierarchy levels (the number of bits (primitives, rows in a cover table) of the qubit variable) multiplied by the time the of the single vertex analysis: $T = \log_2 2^n \times t = t \times n$. The length of the row m of the cover table does not affect to the performance evaluation. The graph vertex analysis includes two kinds of command: the logical (and, or, xor) and a calculating test coverage quality operation that is implemented by applying and-reduction function to all bits of the result vector:

$$m_{ir,j} = M_{i,j} \vee M_{r,j}, (j = \overline{1,n}; \{i \neq r\} = \overline{1,m};);$$

$$m_{ir}^{s} = \wedge m_{ir,j} = \wedge(M_{i,j} \vee M_{r,j})$$

The cost of the hardware implementation of the QH-processor depends of the number of the Hasse diagram vertices and the number of the row cover bits: $H = 2^n \times k \times m$, where k - coefficient of hardware implementation (complexity) of one bit of a binary vector operation and the subsequent calculation of the command coverage quality. Thus, high performance of the coverage problem solutions is achieved by a significant increase of hardware cost (in $2^n \times k \times m / k \times m \times n = 2^n / n$ time compared to the sequential processing of graph nodes) that provides a compromise between fully parallel structure of computational processes (here the cost of equipment depend of the number of primitives in each vertex $H = k \times m \times n \times 2^n$, and the increase of equipment is equal 2^n time) and sequential evaluation uniprocessor computer (here Hasse diagram performance is equal $T = t \times 2^n$, and well as hardware cost is equal $H^* = k \times m \times n$).

Reducing hardware size in comparison with the parallel version of graph processing is $Q^H = k \times m \times n \times 2^n / k \times m \times 2^n = n$ times. The result of the significant hardware redundancy is vertex analysis time reduction in compared to sequential structure and it has the following estimate:

$$Q^T = \frac{t \times 2^n}{t \times n} = \frac{2^n}{n}.$$

Thus, the hardware-oriented model of concurrent boolean calculating (the set of all subsets) on the universe of the n primitives for coverage minimization of Boolean functions, data compression, analysis and synthesis of digital systems through the implementation of the processor structures in the form Hasse diagram is described above. The prototype of a quantum device, implemented on the basis of programmable logic devices for optimal coverage problem solution in the cyberspace analysis is presented in Section 4.

II. WINDOWS-DECOMPOSITION METHOD TO SOLVE THE COVERAGE PROBLEM

The matter of the problem is the large dimension cover table, for example 1000x1000, in this case it is almost impossible to process the optimal coverage solution that has exponential complexity in reasonable period of time. So it is necessary to use optimization approach that can significantly reduce the time and make it acceptable to the practice. Below there are several strategies that allow reducing the time spent to process the large dimension cover tables.

1. Method of the cover table decomposition by string slices

$$C = \{C_1, C_2, ..., C_i, ..., C_n\}, C_i = (C_{i1}, C_{i2}, ..., C_{ij}, ..., C_{im}).$$

Each segment contains m lines, provided that the dimensions of the table and the segment are equal $|C| = n \times m \times k$ and $|C_{ij}| = m \times k$, respectively. Here m is the number of rows in the segment or the number of variables in the Hasse processor, k is the length of the string in the cover table that has to be processed in parallel, n is the number of segments. Disjunction operation is performed on all rows in each segment and after that the table dimension is lowered to m times. If the dimension of the resulting segment table is more than the number of inputs Hasse processor, then it is again the procedure of decomposition. Thus, the original table into a multi-layered cover pyramid, where the upper size is determined by the number of lines, no more than the amount of the inputs of the Hasse processor. For example, if the processor has 8 variables to process concurrently the eight rows of the cover table, the previous (lower) levels should be increased by 8 times (Fig. 2 a). It takes only 5 cycles of matrix multiprocessor Hasse system to process concurrently the table with dimension 32768x3276. At each level the segments that are involved in the higher level declared coverage formation are selected. Keep in mind that pre-segmentation of whole cover space rows is performed until the last level will have the number of segments less or equal to eight (Fig. 2 b).

Level	m
1	8
2	64
3	512
4	4096
5	32768
...	...

a

Level	m
1	32768
2	4096
3	512
4	64
5	8

b

Fig. 1. Quantum structure computing processes

At each level the vector coverage quality of the higher level segments is computed. Vector operation or is used as it is showed below: $C_{ij} = \bigoplus_{r=1}^{k} C_{ijr}$. For example, the coverage table with the dimension 16 to 16

M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
a	1	.	.	.	.	.	.	.	1	.	.	.	.	.	.	1
b	.	.	1	.	.	.	1	.	.	.	.	.	1	.	1	.
c	1	.	.	.	1	.	.	.	.	.	1	.	.	.	.	.
d	.	.	.	1	.	.	.	1	.	.	1	.	.	.	.	.
e	.	.	.	.	1	.	.	.	1	.	.	.	.	1	.	.
f	1	.	1	.	.	.	1	.	.	.	.	.	.	1	.	1
g	.	.	.	1	.	.	.	1	.	.	.	.	.	.	.	.
h	.	.	1	.	1	.	.	.	1	.	1	.	1	.	1	.
i	1	.	1	.	.	1	.	.	1	.	.	.	.	.	.	1
j	1	.	.	1	.	.	.	1	.	.	.	1	.	.	.	.
k	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
l	.	1	.	1	.	.	.	.	1	.	1	.	.	.	.	.
m	1	.	.	.	1	1	.	.	.	.	.	.	1	.	.	.
n	1	.	1	.	.	.	.	.	.	.	.	.	.	.	.	.
p	.	.	.	.	.	.	.	.	.	.	1	.	.	.	.	.
q	.	.	.	1	.	1	.	1	1	.	.	.	.	.	1	.

has to be divided into 4 segments, where each of them consists of four vectors:

M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
a	1	.	.	.	.	.	.	.	1	.	.	.	.	.	.	1
b	.	.	1	.	.	.	1	.	.	.	.	.	1	.	1	.
c	1	.	.	.	1	.	.	.	.	.	1	.	.	.	.	.
d	.	.	.	1	.	.	.	1	.	.	1	.	.	.	.	.
e	.	.	.	.	1	.	.	.	1	.	.	.	.	1	.	.
f	1	.	1	.	.	.	1	.	.	.	.	.	.	1	.	1
g	.	.	.	1	.	.	.	1	.	.	.	.	.	.	.	.
h	.	.	1	.	1	.	.	.	1	.	1	.	1	.	1	.
i	.	.	1	.	.	1	.	.	1	.	.	.	.	.	.	1
j	.	.	.	1	.	.	.	1	.	.	.	1	.	.	.	.
k	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
l	.	1	.	1	.	.	.	.	1	.	1	.	.	.	.	.
m	.	.	.	.	1	1	.	.	.	.	.	.	1	.	.	.
n	.	.	1	.	.	.	.	.	.	1	.	.	.	.	.	.
p	.	.	.	.	.	.	.	.	.	.	1	.	.	.	.	.
q	.	.	.	1	.	1	.	1	1	.	.	.	.	.	1	.
	1	.	1	1	1	.	1	1	1	.	1	.	1	.	1	1
	1	.	1	1	1	.	1	1	1	.	1	.	1	1	1	1
	.	1	1	.	.	1	.	1	1	.	1	1	.	.	.	1
	.	.	1	1	1	1	.	1	1	1	1	.	1	.	1	.

After that, the disjunction of all the s-vectors of each segment is processed, and the result is stored in the (s +1)-vector of the corresponding segment. Then all these vectors are used to solve the coverage problem, but at the higher hierarchy level.

2. The decomposition method for two-dimensional table coverage segments.

M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
a	1	.	.	.	.	.	.	.	1	.	.	.	.	.	.	1	.	.	.	.	.	1	.	.
b	.	.	1	.	.	.	1	.	.	.	.	1	.	1	.	.	.	.	.	.	.	.	.	1
c	1	.	.	.	1	.	.	.	.	.	1	.	.	.	.	.	.	.	.	.	1	.	.	.
d	.	.	.	1	.	.	.	1	.	.	1	.	.	.	.	.	1	.	.	.	1	.	.	.
e	.	.	.	.	1	.	.	.	1	.	.	.	.	1	.	.	.	.	.	.	.	.	.	.
f	1	.	1	.	.	.	1	.	.	.	.	.	.	1	.	1	.	.	.	1	.	.	.	.
g	.	.	.	1	.	.	.	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	.
h	.	.	1	.	1	.	.	.	1	.	1	.	1	.	1	.	.	.	.	.	.	.	.	1
i	.	.	.	.	.	1	.	.	.	.	.	.	.	.	.	1	.	.	.	.	.	1	.	.
j	.	.	.	.	.	.	.	1	.	.	.	1	.	.	.	.	.	.	.	.	.	.	.	.
k	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	.	.	.	.	.
l	.	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	.	.	.	.
m	.	.	.	.	.	1	.	.	.	.	.	1	.	.	.	.	.	.	.	1	.	.	.	1
n	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	.	.	.	1	.	.
p	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	.	.	.	.	.	.
q	.	.	.	.	.	1	.	1	.	.	.	.	.	.	1	.	.	.	.	.	.	.	1	.
r	1	.	.	.	.	.	.	1	.	.	1	.	1	.	.	1	.	.	.	.	1	.	.	.
s	.	1	1	.	.	1	.	.	1	.	1	.	1	.	.	.	.	.	1	.	.	.	.	.
t	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
u	.	1	.	.	.	.	.	.	.	.	1	.	.	.	.	1	.	1	.	.	.	.	.	.
v	.	.	.	.	.	.	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
w	1	.	1	.	1	.	.	.	1	.	.	1	1	.	.	.	.	.	1	.	.	.	.	.
x	.	.	.	.	.	.	.	.	.	1	.	.	.	.	.	.	.	.	.	.	.	.	.	.
y	.	1	.	.	.	.	.	1	1	.	.	.	1	.	.	.	.	.	.	1	.	.	.	.
q1	1	.	1	1	1	.	1	1	1	.	1	.	1	1	1	1	1	.	.	1	1	1	1	1
q2	.	1	.	.	.	1	.	1	.	.	.	1	1	.	1	1	.	1	1	1	.	1	1	1
q3	1	1	1	.	1	1	.	1	1	1	1	.	1	1	.	1	.	1	1	1	1	.	.	.

After the window partition is finished, (s +1, t +1)-vectors are calculated basing on vector disjunction through all s-t-vectors of each window, and the result is stored in (s +1, t +1)-vector of the corresponding (s + 1, t +1)-window. Then all these vectors are used to solve the covering problem at a higher level of the (s +1, t +1)-vectors.

The partition of the table to the segments and the windows has benefits of decreasing in time of the problem solution through the parallel approach where all segments (windows) are processed simultaneously. The drawback is the quasi-determined solution that may differ from the minimum coverage. Below there are the numerical estimates of the costs and benefits of the implementation of two strategies of the proposed optimization method:

$$H^r = \frac{2^n}{(2^{n_1} + 2^{n_2} + ... + 2^{n_i} + ... + 2^{n_k}) + 2^{n/u}}$$

$$H^u = \frac{2^n}{[(2^{n_1} + 2^{n_2} + ... + 2^{n_i} + ... + 2^{n_k}) + 2^{n/u}] \times \frac{r}{u}}$$

$$n = 1000; n_1 = n_2 = ... = n_i = ... = n_{10} = 10; \; r = 1000; u = 100 \rightarrow$$

$$H^r = \frac{2^{1000}}{10 \times 2^{100} + 2^{1000/100}} = \frac{2^{1000}}{10 \times 2^{100} + 2^{10}}$$

$$H^u = \frac{2^{1000}}{(10 \times 2^{100} + 2^{1000/100}) \times \frac{1000}{10}} = \frac{2^{1000}}{1000 \times 2^{100} + 100 \times 2^{10}}$$

Here, the first estimate is the timing cost gain of the solution the coverage problem throgh partitioning the table into k segments, and the second estimate is the gain when string with length r, is divided into segments with length u, that is equal to the number of segments $\frac{r}{u}$. Profit generated by the simultaneous processing of segments or windows. After that, the problem is reduced to covering the segment table. Then an exact result that consist of the strings of segments involved in the cover of the original table is formed of. This method is focused on concurrent processing of all quadrants (windows) by Hasse-processor, the number of them is determined by the number of quadrants. Thus, the cost of the high performance of the concurrent processing is hardware redundancy, depending on the number of windows on the lowest level of the hierarchy table cover.

III. Hardware implementation of QH-processor

A software generator for creating the Verilog code of the Hasse multiprocessor models with different configuration parameters is designed. As input data generator use: the number of input vectors, their length in bits. The program is written on Python 2.7 programming language, and contains 255 lines of code.

The class structure that is designed by the ArgoUML software tools is shown in Fig. 3.

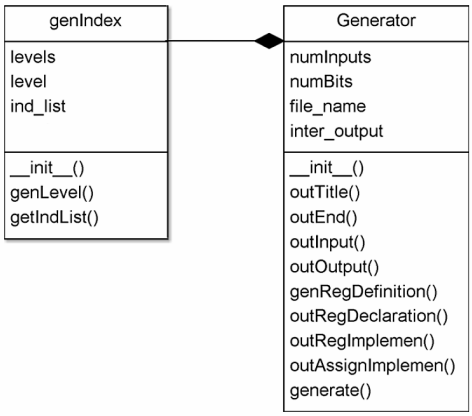


Fig. 3. The class structure of the program (ArgoUML)

It includes the main class Generator, as well as indices of internal registers generator model, that is selected in a separate class genIndex.

The genIndex class has variables: levels is the number of levels in the model (corresponding to the number of Hasse processor inputs), level is the current level of the index register generate, ind_lisc is the list of string values of the indices. The class has two methods: genLevel () and getIndList () which generates and returns a list of indices. Objects of the genIndex class are used in the methods of the Generator class that create descriptions and implementations of the registers.

The Generator class has variables: numInputs is the input number of the Hasse processor model, numBits is the length of the input / output vectors, file_name is file name of the model, inter_output may be equal “True” or “False” and allows to disable the generation of attribute outputs for registers internal levels. Initialization method sets the variables their default values.

def __ init__ (self, numInputs = 4, numBits = 8, file_name = "model.v", inter_output = True):

Any of the parameters can be changed during creation of the Generator class instance, for example:

numInputs = 16

numBits = 8

obj1 = Generator(numInputs, numBits, "model"+str(numInputs)+".v", False).

Functional parts that form the Verilog model of the processor are shown in Fig. 4.

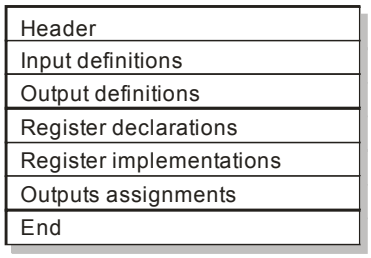


Fig. 4. Verilog model structure of the processor

For implementation of the each part of the model following Generator class methods were designed:

outTitle(), outInput(), outOutput(), outRegDeclaration(), outRegImplemen(), outAssignImplemen() and outEnd(), respectively. Method genRegDefinition(name1, name2, vec = True) is called by outRegDeclaration(). Method generate() that uses the other methods of the class to perform generation of the whole model and write it to a file. In addition the outTitle() and outEnd() functions open and close the external file also.

```
def outTitle(self):
    self.f = open(self.file_name, 'w')
    self.f.write("module device\n  (input clk, rst,\n")
def outEnd(self):
    self.f.write("\nendmodule")
    self.f.close()
```

Tab. 1 illustrates how the device external line number is increased according to rising of the number of the inputs (numInputs). It is obvious that the number of the input signal bits (numBits) doesn't significantly effect on the total number of the inputs and outputs of the model.

TABLE 1

THE DEPENDENCE OF THE OUTPUT NUMBER ON THE INPUT NUMBER (NUMINPUTS) AND THEIR LENGTH (NUMBITS)

numInputs	numBits							
	4	8	12	16	20	24	28	32
4	31	55	79	103	127	151	175	199
6	83	115	147	179	211	243	275	307
8	279	319	359	399	439	479	519	559
10	1 051	1 099	1 147	1 195	1 243	1 291	1 339	1 387
12	4 127	4 183	4 239	4 295	4 351	4 407	4 463	4 519
14	16 419	16 483	16 547	16 611	16 675	16 739	16 803	16 867
16	65 575	65 647	65 719	65 791	65 863	65 935	66 007	66 079
18	262 187	262 267	262 347	262 427	262 507	262 587	262 667	262 747

The model of the device that has 16 inputs, where the length of each input is 8 bits, is implemented using Xilinx Spartan-3E chip: xc3s1200e.

In this case, the resulting circuit contains 3337 flip-flop FF and 3233 4-input lookup tables LUT:

```
Logic Utilization:
  Number of Slice Flip Flops:          3,337 out of  17,344   19%
  Number of 4 input LUTs:              3,233 out of  17,344   18%
```

The generated Verilog code of the 16 input quantum processor has 288,738 lines (16 kb) Based on the results of static timing analysis (Fig. 5), the minimum operating cycle time is equal 9.2 ns that corresponds to 108 MHz frequency.

```
Clock clk to Pad
------------+------------+------------------+--------+
            | clk (edge) |                  | Clock  |
Destination |   to PAD   |Internal Clock(s) | Phase  |
------------+------------+------------------+--------+
o15<0>      |    7.280(R)|clk_BUFGP         |   0.000|
o15<1>      |    7.512(R)|clk_BUFGP         |   0.000|
o15<2>      |    6.999(R)|clk_BUFGP         |   0.000|
o15<3>      |    8.072(R)|clk_BUFGP         |   0.000|
o15<4>      |    7.866(R)|clk_BUFGP         |   0.000|
o15<5>      |    8.242(R)|clk_BUFGP         |   0.000|
o15<6>      |    7.884(R)|clk_BUFGP         |   0.000|
o15<7>      |    9.186(R)|clk_BUFGP         |   0.000|
o16         |    7.680(R)|clk_BUFGP         |   0.000|
------------+------------+------------------+--------+

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    4.250|         |         |         |
---------------+---------+---------+---------+---------+
```

Fig. 5. Time parameters of the 16-input Hasse processor

The GUI of the program code generator that was designed to generate scalable Hasse multiprocessor models is shown in Fig. 6.

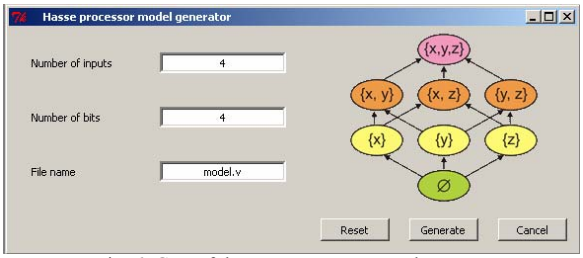
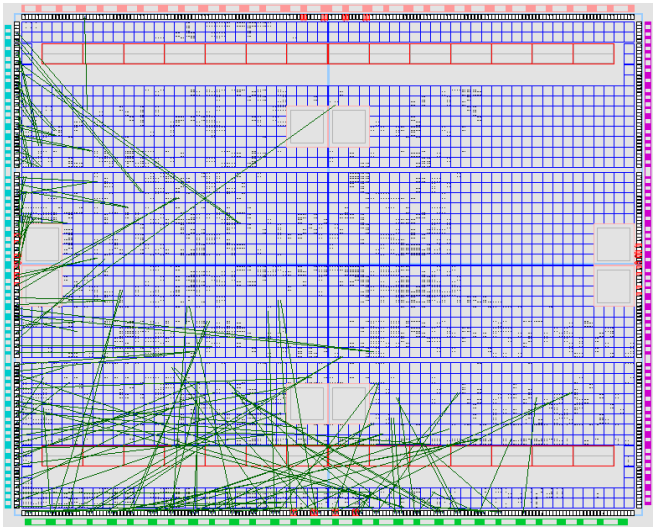


Fig. 6. GUI of the Hasse processor code generator

The synthesis and the implementation of the Hasse processor model was done using open software ISE from Xilinx Inc. The result of its work for 5.5 hours on the Intel processor, 2.1 GHz, is presented in the form of circuit topology xc3s1200e two components at Fig. 7: a) the general plan chips after the Place & Rout procedures of the Implementation stage; b) enlarged fragment of the chip, namely the lower left corner.



a

b

Fig. 7. Placing the device in the chip xc3s1200e: the general plan (a), enlarged fragment (lower left corner) of the chip (b)

IV. Conclusion

The scientific innovation lies in the proposed qubit data structure and quantum model of computational processes, which are based on the use of the Hasse diagram and allow improving significantly (x10-x100) performance of the discrete optimization problem solving. The quasi-optimal method for solving the coverage for large dimension tables was proposed, it differs from the analogue ones due to it has the preliminary phase of the matrix decomposition into segments or windows that allows significant reduction of searching time by applying the parallel register logical operations on the rows of the table. The hardware-oriented model of concurrent (one cycle) calculating of the power set (the set of all subsets) on the n primitive universe for solving covering minimization of Boolean functions, data compression, analysis and synthesis of digital systems through the implementation of the Hasse diagram processor structure was described.

The practical importance of the research lies in the following. Hardware Hasse multiprocessor implementation into the chip Xilinx Spartan-3E: xc3s1200e can significantly reduce the optimization problem solution time by concurrent computing the logical vector operations by increasing the number of processing elements and memory that store intermediate data. Automatic code generator is built in an environment Python significantly reducing (x3 x5) the Verilog code design time and create scalable Hasse processor models for subsequent implementation in Xilinx FPGA chip.

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Method of Pentest Synthesis and Vulnerability Detection

Iryna Hahanova

Abstract – **The structural method for penetration test generation and vulnerability simulation for infrastructure of telecommunication hardware- software information cybernetic systems (CS), focused to protect against unauthorized access the services defined in the system specification by means of penetrating through legal interfaces of component interaction, which have vulnerabilities, is proposed. A protection service infrastructure is created with cybersystem and maintains it during the life cycle, serving all subsequent CS modifications, and constantly improving its intelligence by enlarging the history and libraries of constructive and destructive components.**

I. Introduction

The notions defined by the words "penetration" and "vulnerability" are complementary to each other. If there is vulnerability, the destructiveness that corresponds to the cybersystem functionality may penetrate into it like as the hole. The converse is true, if the penetration was detected, it happened due to vulnerability (hole). The problem of cyberspace protection against unauthorized access lies in "impossible" distinguishing the notions "destructiveness" and "constructiveness" or a valid user. However, there are techniques, technologies, software and systems for effective protecting of corporate or personal cyberspace with a given probability of penetration. The following notions are used in existing publications in this field [1-10]. Penetration test is a set of internal and external destructive impacts focused to detect access vulnerabilities for CS services by means of simulation or analysis of penetrations on cybersystem models. The quality of the test is determined by its fullness, expressed as a percentage, relative to test all the possible types of vulnerabilities, generated manually or automatically for each specific cybersystem. The result of testing the real system (System Under Penetration Test – SUPT) forms a quantitative assessment of the vulnerability, and a list of structural vulnerabilities of pre-assigned types, detected during test experiment. If the testing process has detected non-empty list of destructiveness (vulnerabilities), it is necessary to perform diagnosis based on diagnostic tests to determine the location, cause and kind of the vulnerability with a given depth for searching destructiveness. After reveal of all vulnerabilities their removing is performed through partial or complete reconstruction of cybersystem by using proven library structural solutions. All described above procedures use three libraries: 1) negative one, describing all the possible types of vulnerabilities; 2) positive one, where each vulnerability is associated with hardware and software solutions to remove the destructiveness; 3) unproven solutions – the "intelligence" of CS that can be redefined when functioning cybersystem. All three libraries must be updated when designing and utilizing cybersystem in real time.

Objectives of the infrastructure for protecting cybersystem are:

1) Synthesis of CS deductive model for testing, diagnosis, and repairing invulnerability of cybersystem [1,2];

2) Generating test patterns for checking and diagnosing vulnerabilities, which are close to 100% coverage.

3) Creating a vulnerability detection algorithms with given diagnosis granularity.

4) Creating test generators for checking and diagnosing vulnerabilities, which are close to 100% coverage.

5) Testable design (modification) of invulnerable cybersystems free from the vulnerabilities at the current state of technological and mathematical culture.

6) Development of embedded infrastructure for protecting cybersystem, focused to monitoring, testing, diagnosis and repairing invulnerability in real time during the operation.

7) Development of specialized algorithms and plans for monitoring, testing, diagnosis and repairing invulnerability of CS in real time during the operation.

8) Verification of testable infrastructure solutions designed for real CS's.

The object of testing is a cybernetic system of interacting hardware-software, telecommunication, and information components, focused on providing quality services through the standard interfaces to the authorized users in real time. All types of vulnerabilities (penetrations) don't lead the object under test beyond the bounds of given functionality of cybersystem that is described by Boolean function:

$$Y = f(X_1, X_2, ..., X_i, ..., X_n),\ X_i, Y \in \{0,1\}.$$

Therefore, the model of vulnerabilities is applied to graph structure of functional modules with input and output transaction variables. Transaction graph is represented by arcs – functionalities (services) with monitors (assertions) – and nodes, which form the states of cybersystem through variables, memory, interface input-output ports, transceivers, terminals, and computers:

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$F = (A * B) \times S$, where $S = \{S_1, S_2, ..., S_i, ..., S_m\}$ – nodes or state of CS when simulating test segments. Each state $S_i = \{S_{i1}, S_{i2}, ..., S_{ij}, ..., S_{ip}\}$ is determined by the values of essential variables CS (variables, memory, terminals, and computers). Oriented arcs of the graph are the function blocks:

$$B = (B_1, B_2, ..., B_i, ..., B_n), \ \bigcup_{i=1}^{n} B_i = B; \ \bigcap_{i=1}^{n} B_i = \varnothing,$$

where each of them can be associated with assertion $A_i \in A = \{A_1, A_2, ..., A_i, ..., A_n\}$ for monitoring the functionalities in time and space.

There are basic technologies for testing security of cybersystems: OSSTMM – The Open Source Security Methodology Manual; NIST Guideline on Network Security Testing; ISACA Switzerland – Testing IT Systems Security With Tiger Teams; Draft Guideline on Network Security Testing; NIST Special Publication 800-26 Security Self-Assessment Guide for Information Technology Systems; Cybersecurity Vulnerability Assessment Methodologies (Cybersecurity VAMs); Information Systems Security Assessment Framework, OISSG.

II. Apparatus of Boolean derivatives for test synthesis

An apparatus of Boolean derivatives is designed for checking significant variables and components of cybersystem, including significance analysis of destructive components (vulnerability and penetration) for cybersystem state. Methods of taking Boolean derivatives by truth table, disjunctive form or cubic coverage to create conditions for activating the input variables, when synthesizing tests to check the vulnerabilities (penetrations), are proposed. Consideration of the method is performed on following three examples of logic functions: 1) $f(x) = x_1 \vee x_1\overline{x}_2$. 2) $f(x) = x_1x_2 \vee \overline{x}_1x_3$. 3) $f(x) = \overline{x}_2\overline{x}_3 \vee x_1x_2x_3$.

Issues to be addressed: 1) Definition of all derivatives of first-order by analysis, cubic and tabular form of logical functions representation. 2) Verification of activation conditions, obtained by their modeling on one of forms of functionality description. 3) Synthesis of activation tests for variables of logic function on the basis of calculating derivatives.

Example 1. Define all the derivatives of first order by analytical form of logical function $f(x) = x_1 \vee x_1\overline{x}_2$.

Application of calculation formula

$$f'(x_i) = \frac{df(x_1, x_2, ..., x_i, ..., x_n)}{dx_i} =$$

$$= f(x_1, x_2, ..., x_i = 0, ..., x_n) \oplus f(x_1, x_2, ..., x_i = 1, ..., x_n)$$

defines Boolean first derivative as the sum modulo two of zero and unit residual functions.

For the function it is obtained:

$$\frac{df(x_1, x_2)}{dx_1} = f(0, x_2) \oplus f(1, x_2) =$$

$$(0 \vee 0\overline{x}_2) \oplus (1 \vee 1\overline{x}_2) = 0 \oplus 1 = 1;$$

$$\frac{df(x_1, x_2)}{dx_2} = f(x_1, 0) \oplus f(x_1, 1) =$$

$$= (x_1 \vee x_1 \cdot \overline{0}) \oplus (x_1 \vee x_1 \cdot \overline{1}) = (x_1 \vee x_1 \cdot 1) \oplus (x_1 \vee x_1 \cdot 0) =$$

$$= (x_1 \vee x_1) \oplus (x_1 \vee 0) = x_1 \oplus x_1 = 0.$$

Zero value of derivative means the absence of activation conditions of the variable x_2, which allows considering it as insignificant, and therefore to remove it from the number of variables, which form functionality.

Example 2. Define all the derivatives of first order by analytical form of logical function $f(x) = x_1x_2 \vee \overline{x}_1x_3$. For the function the following calculations are performed:

$$\frac{df(x_1, x_2, x_3)}{dx_1} = f(0, x_2, x_3) \oplus f(1, x_2, x_3) =$$

$$= (0 \cdot x_2 \vee \overline{0} \cdot x_3) \oplus (1 \cdot x_2 \vee \overline{1} \cdot x_3) =$$

$$= (0 \vee 1 \cdot x_3) \oplus (x_2 \vee 0 \cdot x_3) =$$

$$= x_3 \oplus x_2 = x_2\overline{x}_3 \vee \overline{x}_2x_3;$$

$$\frac{df(x_1, x_2, x_3)}{dx_2} = f(x_1, 0, x_3) \oplus f(x_1, 1, x_3) =$$

$$= \overline{x}_1x_3 \oplus (x_1 \vee x_3) =$$

$$= \overline{\overline{x}_1x_3}(x_1 \vee x_3) \vee \overline{x}_1x_3\overline{(x_1 \vee x_3)} =$$

$$= (x_1 \vee \overline{x}_3)(x_1 \vee x_3) \vee \overline{x}_1x_3\overline{x}_1\overline{x}_3 = x_1;$$

$$\frac{df(x_1, x_2, x_3)}{dx_3} = f(x_1, x_2, 0) \oplus f(x_1, x_2, 1) =$$

$$= x_1x_2 \oplus (\overline{x}_1 \vee x_2) =$$

$$= \overline{x_1x_2}(\overline{x}_1 \vee x_2) \vee x_1x_2\overline{(\overline{x}_1 \vee x_2)} =$$

$$= (\overline{x}_1 \vee \overline{x}_2)(\overline{x}_1 \vee x_2) \vee x_1x_2x_1\overline{x}_2 = \overline{x}_1.$$

For three variables 4 activation conditions are obtained, which correspond to four logical paths in the circuit structure of disjunctive form of the function.

Example 3. Define all the derivatives of first order by cubic form of logical function

$f(x) = \overline{x}_2\overline{x}_3 \vee x_1x_2x_3 =$

x_1	x_2	x_3	Y
X	0	0	1
1	1	1	1
X	0	1	0
X	1	0	0
0	1	X	0

=

$=$

$\frac{x_2x_3}{x_1}$	00	01	11	10
0	1	0	0	0
1	1	0	1	0

$=$

x_1	x_2	x_3	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

The process model for calculating the derivative by the variable x_i for the function, given in tabular form, includes the following steps: 1) Simulating of input patterns by the truth table (cubic coverage), to determine the column Y_i^0, where the variable x_i, has only zero value for all rows of the truth table. The number of such patterns is always $q = 2^{n-1}$, n – a number of variables. 2) Calculating coordinates of the column Y_i^1, with unit value of variable x_i for all rows of the table. 3) Calculating the column $Y_i^{\oplus} = Y_i^0 \oplus Y_i^1$ subject to rule $0 \oplus X \vee 1 \oplus X = X$. 4) Forming disjunctive form of function derivative by unit values of the column $Y_i^{\oplus}$ without the variable x_i, at which the derivative is taken. Otherwise, the table rows, corresponding to unit values of the column $Y_i^{\oplus}$, defining the derivative of the function, are fixed. The analytical model of taking the derivative of the function, represented in tabular form, is as follows:

$$\frac{df}{dx_i} = f(x_1, x_2, ..., x_i = 0, ... x_n) \oplus f(x_1, x_{2,...,} x_i = 1, ... x_n);$$

$$Y_i^{\oplus} = [Y_i^0 = f(x_1, x_2, ..., x_i = 0, ..., x_n)] \oplus [Y_i^1 = f(x_1, x_{2,...,} x_i = 1, ..., x_n)].$$

Lemma of non-intersection cubes. The possibility of correct taking the derivative for obtaining activation test on the variable x_i is limited by minimum structure of cubic coverage or analytical disjunctive (conjunctive) normal form, where intersection of any cubes (rows of the truth table), or terms of DNF (CNF) gives empty set:

$$\frac{df}{dx_i} = f(x_1, x_2, ..., x_i = 0, ... x_n) \oplus f(x_1, x_{2,...,} x_i = 1, ... x_n) \in T \leftrightarrow$$

$$\forall i, j (C_i \cap C_j = \varnothing);\ i, j = \overline{1, n};\ i \neq j.$$

In fact, if the coverage described above, to define according the rules of non-intersection cubes, all derivatives will be valid for test synthesis without additional check:

$f(x) = \bar{x}_2\bar{x}_3 \vee x_1x_2x_3 =$

x_1	x_2	x_3	Y
X	0	0	1
1	1	1	1
X	0	1	0
X	1	0	0
0	1	X	0

$\rightarrow$

x_1	x_2	x_3	Y
X	0	0	1
1	1	1	1
X	0	1	0
X	1	0	0
0	1	1	0

To get the cubic coverage it is necessary to perform minimization by all the existing methods (maps Karnaugh, Quine, essential variables, undetermined coefficients, binary graph) subject to the rule: coverage of zero and unit coordinates of the truth table should not be intersected during minimization. In the present case, when the functionality is rewritten subject to this rule, even the total number of cubes is not changed, while the coverage acquired the quality of non-intersection (as a truth table) for synthesizing test of activation variables:

$\frac{df}{dx_1} =$

x_1	x_2	x_3	Y	Y_2^0	Y_2^1	$Y_2^{\oplus}$
X	0	0	1	1	1	0
1	1	1	1	0	1	1
X	0	1	0	0	0	0
X	1	0	0	0	0	0
0	1	1	0	0	0	0

$= x_2x_3;$

$\frac{df}{dx_1} =$

x_1	x_2	x_3	Y	Y_2^0	Y_2^1	$Y_2^{\oplus}$
0	0	0	1	1	1	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	1	0
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	1	1

$= x_2x_3.$

Calculation of derivatives in all input variables makes it possible to construct an activation test for functionality, defined by not truth table, but a cubic coverage that can considerably reduce the time of test synthesis.

Thus, all the results of calculating the derivatives by using three forms of function definition are identical. The method for taking the derivative by the truth table is the most technological. But the use of a cubic coverage has lower computational complexity because of compact representation of the functionality when introducing redundancy (symbol X) in a binary alphabet. Using the analytical form leads to significant increase in the complexity of the algorithms associated with application the laws of Boolean algebra and function minimization, which limits its application when solving practical problems.

The process model for obtaining the test $T = [T_{ij}],\ i = \overline{1, k};\ j = \overline{1, n}$ of combinational function is:

1) $f'(x_i) = f(x_1, x_2, ..., x_i = 0, ..., x_n) \oplus f(x_1, x_{2,...,} x_i = 1, ..., x_n)$;

2) $T = \bigcup_{i=1}^{n} [f'(x_i) * (x_i = 0) \vee (x_i = 1)]$;

3) $T_{ij} = T_{i-1,j} \leftarrow T_{ij} = X$; $T_{1j} = 1 \leftarrow T_{1j} = X$;

4) $T = T \setminus T_i \leftarrow T_i = T_{i-r}$, $r = \overline{1, i-1}$, $i = \overline{2, n}$.

1) Calculating the derivatives for all n variables of the functionality by using one of the forms: analytical, tabular, or cubic. 2) Combining all conditions (vectors) of activation in a table, where each vector is associated by means of concatenation (*) with change of the variable on which the derivative was taken, which means doubling the number of test patterns with respect to the total quantity (k) of activation conditions. 3) Extending the definition of the symbol X = {0,1} of the coordinate by assigning a binary value of the same coordinate in the previous vector for obtaining the test of the minimum length. 4) Minimization of test vectors by removing repeated input sequences.

Fig. 2 illustrates the tables for test obtaining the in accordance with items 2-4 of the algorithm for the functionality $f = \bar{x}_2 \bar{x}_3 \vee x_1 x_2 x_3$ provided by the circuit structure.

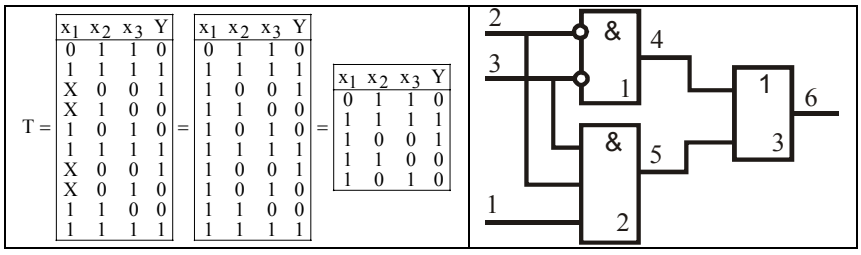

Fig. 2. Test tables and circuit structure of Boolean function

The resulting test is identical by quality and quantity with the input patterns, previously synthesized by the method $F \oplus L$, therefore, it is characterized by the same properties of fault coverage and depth of vulnerability detection.

The proposed process model for synthesizing tests when testing and diagnosing vulnerabilities can be used as an embedded component of CS infrastructure IP.

III. Deductive method for vulnerabilities in CS detection

The main idea of the deductive method is to analyze the mapping of input and output data of cybersystem in order to detect destructive penetrations or vulnerabilities by performing comparison between well-known (functional) modes and situations which cause suspicion. For the implementation of the method in the infrastructure of protective services it is necessary to have graph model of cybersystem functional logic, which simply can be transformed to a system of logical equations, suitable for deductive analysis. Further, it is proposed a model for deductively parallel synchronous analyzing vulnerabilities (penetrations) in cybersystem (object), which allows calculating all destructive components, detectable by a test vector, for one iteration of processing the structure. The aim of deductive analysis is to determine the quality of the synthesized test concerning the completeness of vulnerability coverage, and build a table for checking by test patterns all detected vulnerabilities of CS to perform the diagnosis procedures. This model is based on solving the equation:

$$L = T \oplus F, \qquad (1)$$

where $F = (F_{m+1}, F_{m+2}, ..., F_i, ...F_n)(i = \overline{m+1, n})$ is a set of vulnerability-free (correct) behavior functions CS; m is a number of inputs; $Y_i = F_i(X_{i1}, ..., X_{ij}, ..., X_{in_i})$ – n_i-input i-th circuit element that realizes F_i to determine the state of the line (output) Y_i on test vector T_t; here X_{ij} – j-th input i-th element; test $T = (T_1, T_2, ..., T_t, ..., T_k)$ is an ordered set of binary vectors, extended during vulnerability-free simulation on a set of input, internal and output lines, combined in the matrix

$$T = [T_{ti}] = \begin{bmatrix} T_{11}, T_{12}, ..., T_{1i}, ..., T_{1n} \\ ..... \\ T_{t1}, T_{t2}, ..., T_{ti}, ..., T_{tn} \\ ..... \\ T_{k1}, T_{k2}, ..., T_{ki}, ..., T_{kn} \end{bmatrix}, \qquad (2)$$

not input coordinates of which is defined by simulating the function $T_{ti} = Y_i = F_i(X_{i1}, ..., X_{ij}, ..., X_{in_i})$ on the test vector T_t; $L = (L_1, L_2, ..., L_t, ..., L_k)$ is a set of deductive circuits or models, which are defined by expression (3), where $L_t = (L_{t1}, L_{t2}, ..., L_{ti}, ..., L_{tn})$;

$$L_{ti} = T_t \oplus F_i \qquad (3)$$

– deductive function (DF) of parallel vulnerability simulation on test vector T_t, corresponding vulnerability-free element F_i, which makes it possible to calculate the list of input penetrations transported to the output of the element F_i [8].

The concept of synchronism of the proposed model (1) is defined by the following condition: $\Delta t = (t_{j+1} - t_j) >> \tau >> \tau_i$, when time interval between changing of the input vectors $(t_{j+1} - t_j)$ much greater than the maximum delay of the system τ and element τ_i. This makes it possible to exclude time as insignificant parameter [8], which is used in the technologies of simulation and test synthesis.

In general, when a function of CS is represented by the truth table, the application of the formula (1) allows obtaining for a given test vector T_t a vulnerability (penetration) transportation table, on which we can write DF for simulating destructiveness. Examples for such functions are presented in the following form (the first term is a test vector, the second one and the result - a truth table and vulnerability transportation table):

X_1	X_2	Y_1
0	1	0

$\oplus$

X_1	X_2	Y_1
0	0	0
0	1	0
1	0	1
1	1	1

$=$

X_1	X_2	L_1
0	1	0
0	0	0
1	1	1
1	0	1

$L_1 = X_1X_2 \vee X_1\overline{X}_2;$

X_1	X_2	Y_2
1	1	1

$\oplus$

X_1	X_2	Y_2
0	0	0
0	1	0
1	0	0
1	1	1

$=$

X_1	X_2	L_2
1	1	1
1	0	1
0	1	1
0	0	0

$L_2 = X_1X_2 \vee X_1\overline{X}_2 \vee \overline{X}_1X_2.$

Here the deductive functions L_1, L_2 are written in a disjunctive normal form by constituents of "1" of destructiveness transportation table. Whereas division of the test on vector components the equation (1) for obtaining DF for $T_t \in T$ takes the form: $L_t = T_t \oplus F$. If functional description of CS is represented by components (primitives), which form the states of all lines (connections) of CS, the following expression is used as transformation formula of vulnerability-free model for the primitive F_i on the test vector T_t to the deductive function L_{ti}:

$$L_{ti} = T_t \oplus F_i = f_{ti}[(X_{i1} \oplus T_{t1}),(X_{i2} \oplus T_{t2}),..., (X_{ij} \oplus T_{tj}),...,(X_{in_i} \oplus T_{tn_i})] \oplus T_{ti}, \quad (4)$$

which is the basis of deductive analyzing the destructive violations of CS [3, 6].

Example 4. Get the deductive functions of parallel simulating vulnerabilities on an exhaustive test for the basis of the functional elements And, Or, Not. Subject to expression (4) the following obvious transformations of the function And are performed:

$$L_{and}[T = (00,01,10,11), F = (X_1 \wedge X_2)] =$$
$$= L\{(\overline{x}_1\overline{x}_2 \vee \overline{x}_1x_2 \vee x_1\overline{x}_2 \vee x_1x_2) \wedge [(X_1 \oplus T_{t1} \wedge X_2 \oplus T_{t2}) \oplus T_{t3})]\} =$$
$$= (\overline{x}_1\overline{x}_2)\{[(X_1 \oplus 0) \wedge (X_2 \oplus 0)] \oplus 0\} \vee (\overline{x}_1x_2)\{[(X_1 \oplus 0) \wedge (X_2 \oplus 1)] \oplus 0\} \vee$$
$$\vee (x_1\overline{x}_2)\{[(X_1 \oplus 1) \wedge (X_2 \oplus 0)] \oplus 0\} \vee (x_1x_2)\{[(X_1 \oplus 1) \wedge (X_2 \oplus 1)] \oplus 1\} =$$
$$= (\overline{x}_1\overline{x}_2)(X_1 \wedge X_2) \vee (\overline{x}_1x_2)(X_1 \wedge \overline{X}_2) \vee (x_1\overline{x}_2)(\overline{X}_1 \wedge X_2) \vee (x_1x_2)(X_1 \vee X_2).$$

Similarly calculations are performed for the function Or:

$$L_{or}[T = (00,01,10,11), F = (X_1 \vee X_2)] =$$
$$= L\{(\overline{x}_1\overline{x}_2 \vee \overline{x}_1x_2 \vee x_1\overline{x}_2 \vee x_1x_2) \wedge [(X_1 \oplus T_{t1} \vee X_2 \oplus T_{t2}) \oplus T_{t3})]\} =$$
$$= (\overline{x}_1\overline{x}_2)\{[(X_1 \oplus 0) \vee (X_2 \oplus 0)] \oplus 0\} \vee (\overline{x}_1x_2)\{[(X_1 \oplus 0) \vee (X_2 \oplus 1)] \oplus 1\} \vee$$
$$\vee (x_1\overline{x}_2)\{[(X_1 \oplus 1) \vee (X_2 \oplus 0)] \oplus 1\} \vee (x_1x_2)\{[(X_1 \oplus 1) \vee (X_2 \oplus 1)] \oplus 1\} =$$
$$= (\overline{x}_1\overline{x}_2)(X_1 \vee X_2) \vee (\overline{x}_1x_2)(\overline{X}_1 \wedge X_2) \vee (x_1\overline{x}_2)(X_1 \wedge \overline{X}_2) \vee (x_1x_2)(X_1 \wedge X_2).$$

Here $T_t = (T_{t1}, T_{t2}, T_{t3}), (t = \overline{1,4})$ is test vector, having 3 coordinates, where the last one defines an output state of two-input element And (Or). In the next transformation $T_t = (T_{t1}, T_{t2}), (t = \overline{1,2})$ is test vector, having 2 coordinates, where the second one defines a state of the inverter output:

$$L_{not}[T = (0,1), F = \overline{X}_1] = L\{(\overline{x}_1 \vee x_1)[(\overline{X_1 \oplus T_{t1}}) \oplus T_{t2}]\} =$$
$$= \overline{x}_1[(\overline{X_1 \oplus 0}) \oplus 1] \vee x_1[(\overline{X_1 \oplus 1}) \oplus 0] = \overline{x}_1\overline{\overline{X}}_1 \vee x_1\overline{\overline{X}}_1 = \overline{x}_1X_1 \vee x_1X_1.$$

The last expression shows the inversion invariance to the input set for vulnerabilities transportation. It transforms into a repeater. So this function does not appear on the outputs of deductive elements. Joint hardware implementation of DF for the remaining two-input elements And, Or on exhaustive test is represented by universal functional primitive (Fig. 3) for deductive-parallel vulnerability analysis.

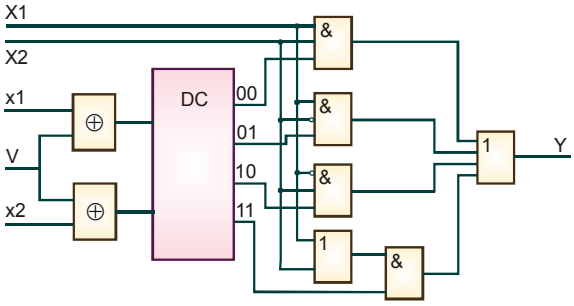

Fig. 3. Simulator of vulnerable primitives

In the simulator there are Boolean (x1, x2) and register (X1, X2) inputs for coding vulnerabilities, the variable for choosing the type of vulnerability-free function (AND, OR), output register variable Y. The states of binary inputs x1, x2 and a variable for choosing the element determine one of four deductive functions for vector Y of testable vulnerabilities.

To illustrate parallel simulation of input 8-bit vectors of vulnerabilities in order to obtain a set of detectable destructive components for logic elements 2And, 2Or on the output Y the following table is used:

(V, x1, x2) =	000	100	011	111	010	110
X1(RG)	01110001	01110001	10110110	00111011	00101010	10111001
X2(RG)	01111000	01111000	10110101	00110100	10111001	00101010
Y(RG)	01110000	01111001	10110111	00110000	10010001	10010001

The use of this simulator allows transforming a functional model F of correct behavior CS to deductive model L, which is invariant in the sense of generality of test sets, and it is not focused on use model F during simulation. Therefore the simulator as hardware model of DF is effective engine for deductive parallel simulation of CS, which increases the speed of cybersystems analysis in 10–1000 times in comparison with the software implementation. But the ratio of model volumes for correct modeling and vulnerability analysis is 1:10. The approach of hardware analysis of destructive components is focused to enhancing the functionality of embedded simulation tools, which can be stored in the clouds, and constantly be used to verify infrastructure of CS protective services. The computational complexity of processing project, consisting of n components, is equal to $Q = (2n^2\tau)/W$, where τ is time for executing the register operation (And, Or, Not); W – the register width.

Thus, method for deductive parallel simulating allows estimating the quality (coverage) of proposed tests, and determining all potential places of existence vulnerabilities and their subsequent elimination.

III. Conclusion

1. Improved methods for test synthesis of functionalities, defined by the matrix form of description of CS component behavior, which differ by parallelism of vector operations on tables that makes it possible to considerably (x2) improve the performance of computational procedures, are developed.

2. Process models and methods for test synthesis of functionality and diagnosing FV can be used as embedded components of the infrastructure IP based on the testability standards.

3. Method for FV deductive parallel simulation allows estimating the quality (coverage) of proposed tests, and determining all potential places of existence vulnerabilities and their subsequent elimination.

4. The feasibility of proposed investigation is to create a formal model for subsequent significant time reduction of existing test methods of diagnosing and fixing vulnerabilities corporate cybernetic system.

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PIN Photodiodes For Gamma Radiation Measurements

M.A. Khazhmuradov, N.A. Kochnev, D.V. Fedorchenko

Abstract – **We consider usage of the commercial PIN photodiodes as detectors for gamma-radiation. We describe the low-noise electronic circuit for detector module using BPW-34 photodiode. Theoretical and experimental results for counting and spectrometry modes using the developed detector module are presented. Parameters of BPW-34 photodiode and compact Geiger-Müller tube are compared.**

I. Introduction

The modern industrial applications of radiation technologies require compact, fast and low cost radiation detectors. For the appliances where spectral measurements are not required the Geiger-Müller tubes are often used. This includes radiation level control, contamination measurements, well logging. The shortcomings of such detectors are well known and include rather low sensitivity especially for compact detectors, limits on count-rate and lifetime, high operational voltage.

The possible alternatives to Geiger-Müller tubes for dosimetry applications are PIN photodiodes. While these silicon detectors are designed to have very high sensitivity to visible light or infrared radiation they are also capable to register X-ray and low energy gamma radiation. Numerous studies of commercial visible light and infrared PIN photodiodes have proved that they could be used for spectrometry and counting applications for photon energies up to 100 keV [1-4]. In the work [2] PIN photodiodes were tested for 661 keV gamma photons and exhibited enough sensitivity for counter applications.

The main purpose of this paper is to study the BPW-34 commercial photodiode as a replacement of compact Geiger-Müller tube. This includes studies of both counting mode and spectrometry mode that is absent in Geiger-Müller tube.

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II. Experimental setup

As radiation detector we have chosen commercial BPW-34 PIN photodiode. This photodiode usually is part of photo-interrupters or infrared control devices.

BPW-34 photodiode was intensively studied in the works [1-4] as gamma radiation detector. This diode has a plastic packaging (see Fig. 1). The sensitive component of the detector is 3×3 mm silicon die placed inside the packaging.

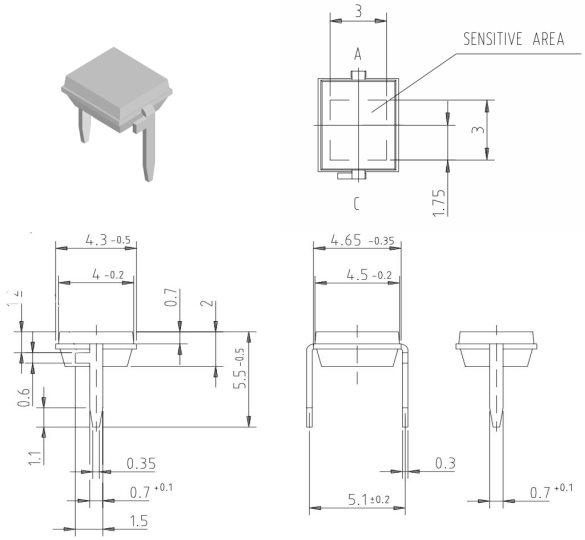

Fig. 1. BPW-34 PIN photodiode

The structure of sensitive area is typical to PIN photodiodes and is shown in the figure 2. It has a thick layer of intrinsic semiconductor i placed between the n and p layers. This layer is the primary region where incident photons are captured and photocurrent is generated. Additional n+ layer improves electric contact between sensitive area and metal electrode.

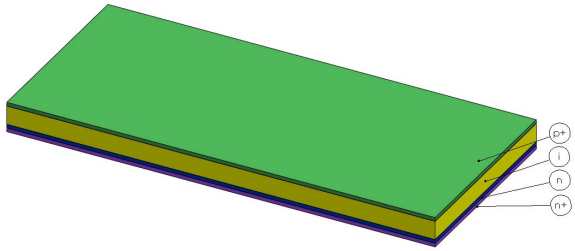

Fig.2. Structure of the sensitive layer

For the BPW-34 photodiode width of the intrinsic layer is 210 μm [4]. When photon is captured in this area charge carriers emerge. The reverse voltage applied to the photodiode drives them to the corresponding conductivity areas. As a result a current pulse is generated.

Generation of the single electron-hole pair requires approximately 3.6 eV. To estimate the typical values of generated charge let us consider full capture of the single 59.2 keV photon that corresponds to the principal line of the 241Am spectrum. In this case the total charge of 2.6 fC is generated in the photodiode.

To register such a low charge one needs a low-noise electronic circuit with high input impedance and low input capacitance. These requirements are satisfied by amplifiers using junction gate field-effect transistors (JFET). We have developed and manufactured electronic circuit for source follower based on low-noise JFET transistor (see Fig. 3). Source follower circuit was chosen due to very low input capacity. In this case under constant gate-source voltage gate-source capacitance becomes zero, and as the drain potential is constant no increase of gate-drain capacitance due to Miller effect occur.

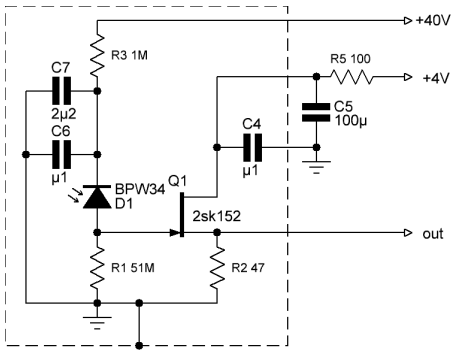

Fig. 3. JFET based source follower circuit

Now we estimate the total input capacitance of the whole circuit. For the low-noise JFET transistors 2SK152 input capacitance is less than 2 pF. Under turn-off voltage of 40 V PBW-34 photodiode has capacitance 10 pF, and with account for stray wiring capacitance the total input capacitance is less than 15 pF. Hence for input charge of 2.6 fC the output pulse amplitude is 0.17 mV.

The output from the source follower is transmitted to the driver amplifier with amplification 2000 and shaping time 50 μs (Fig. 4.). Driver amplifier has three stages: the first is differentiating stage and he second and third stages are integrating stages.

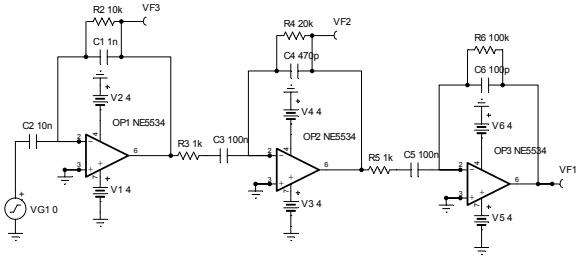

Fig. 4. Driver amplifier circuit

After amplification and sharpening the output signal goes to analog-digital convertor (ADC) and microcontroller circuit. The AD conversion is performed by 10-digit ADC AD9200 and then data is preprocessed by Atmel Mega88PA microcontroller. Every 300 ns microcontroller reads ADC conversion data and determines the pulse maximum and duration. Microcontroller program also performs additional signal filtering from the random noise. After preprocessing microcontroller transmits data to personal computer PC through the UART-USB bridge based on the CP2102 module.

Due to the low input capacitance and very high input impedance the source follower circuit from the figure 3 has high sensitivity to electric interferences. Also it is subjected to microphone effect in photodiode and ceramic capacitors in differentiating and integrating stages. Besides that the circuit exhibits very high sensitivity to visible, infrared and ultraviolet light. Thus we have provided electrical and light shielding of the source follower circuit using the 35 μm copper foil.

III. Mathematical Simulation

From the viewpoint of gamma radiation detection BPW-34 photodiode has relatively low sensitive layer thickness. Additionally, due to low atomic number of silicon the photo effect cross-section is rather low, especially for energies above 100 keV. At the same time registration of such photons is still possible due to the Compton scattering and consequent registration of secondary electrons.

The theoretical studies of the above scattering mechanism were performed using GEANT 4.9.6.1 software [5]. This software was developed by CERN and Geant4 is aimed on the simulation of the passage of particles through matter.

We have developed the solid model for BPW-34 photodiode (Fig. 5).

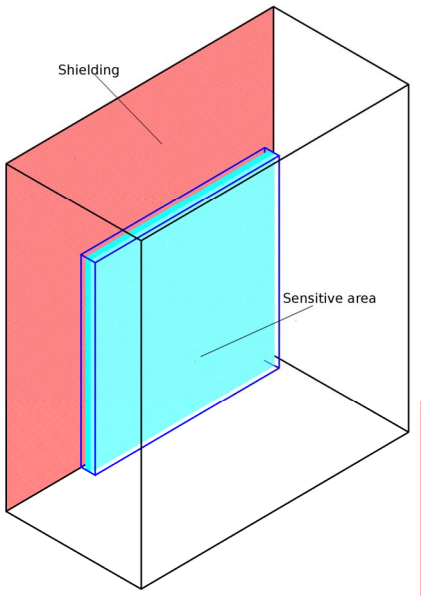

Fig. 5. GEANT4 model of BPW-34 photodiode

It included epoxy case, silicon sensitive area with variable base thickness, and copper shielding with variable thickness. The case was approximated by a solid box with the following dimensions: 4.5×4×2 mm. The size of sensitive area was 2.75×2.75×0.21 mm.

Although it was possible to change the base thickness preliminary simulations showed that for lower width detection efficiency degrades. For the real photodiode base thickness depends on the applied voltage and for 40 V turn-off voltage we have used it has the maximum value of 210μm [4]. The typical shielding thickness used during the simulation was 35 μm.

Within the GEANT 4.9.6.1 framework several models for simulation of photon and electron passage are available. For actual simulation we used G4EmStandardPhysics (option 4) package which includes the most exact models for the electromagnetic processes in the low energy range. Incident photon energy spectra corresponded to the spectra of real radiation sources: ^{137}Cs, ^{179}Ta, ^{241}Am. Radiation properties of these sources are given in the Table I.

TABLE I

Nuclide	Energy, keV	Relative intensity, %	Backscattering energy, keV
^{137}Cs	31,817	2,110	28,294
	32,194	3,850	28,591
	36,304	0,368	31,787
	36,378	0,711	31,844
	37,255	0,225	32,514
	661,000	90,000	184,272
^{179}Ta	54.611	13.818	44.99
	55.79	24.158	45.79
	63.2	8.093	50.67
	65	2.053	51.82
^{241}Am	13.9	12.5	13.183
	17.8	18.0	16.64
	20.8	4.7	19.234
	26.35	2.4	23.887
	59.54	35.9	48.287

For the real-world dosimetry applications detector performance for ^{137}Cs radiation source is of particular interest. We have calculated the energy absorption spectrum for this source (Fig. 6).

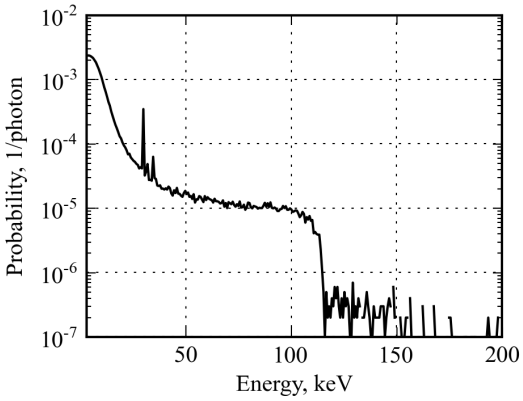

Fig. 6. Calculated energy absorption spectrum for ^{137}Cs

As we have stated above the photo effect cross-section for ^{137}Cs primary line 662 keV is rather low and photodiode detects only secondary electrons from Compton scattering with energies less than 114 keV with constant probability about $1.0 \cdot 10^{-5}$. The calculated total efficiency (ratio of the number of detected photons to the number of incident photons) of the BPW-34 photodiode for ^{137}Cs source is $2.0 \cdot 10^{-3}$. This efficiency is sufficient for counting applications.

At the photon energies less than 60 keV BPW-34 sensitivity is enough both for counting and spectrometry modes. We have calculated energy absorption spectra for ^{179}Ta and ^{241}Am nuclides which were used for experimental measurements. Figures 7 and 8 show the calculated energy absorption spectra.

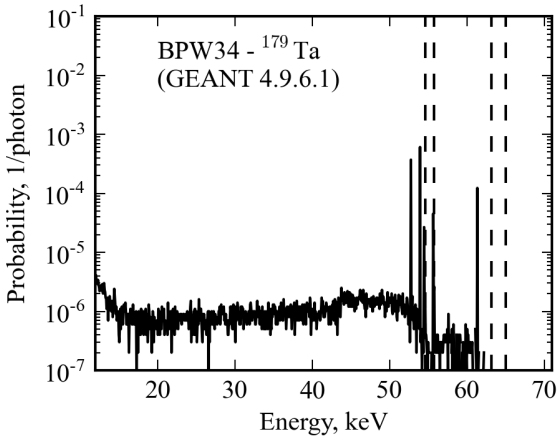

Fig. 7. Calculated energy absorption spectrum for ^{179}Ta

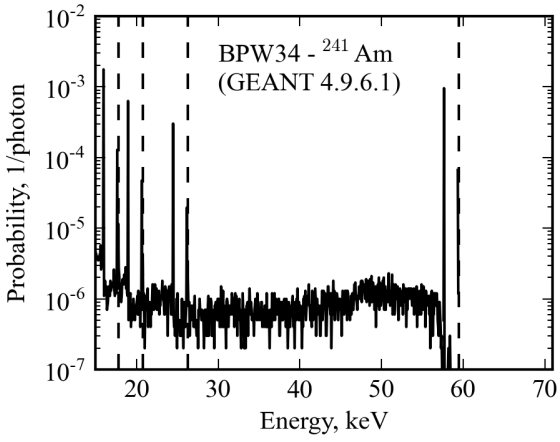

Fig. 8. Calculated energy absorption spectrum for ^{241}Am

In the figures 7 and 8 dashed lines denote spectrum lines for the corresponding nuclide (see Table I). Note that absorption lines are shifted to lower energies. This arises due to photo effect on the K and L shells of the silicon with binding energies 1839 eV for K shell and 149.7 eV, 99.8 eV, 99.2 eV for L_I, L_{II} and L_{III} shells [5].

IV. Results and discussions

For the counting mode measurements we have used the ^{137}Cs source with activity of 55.5 kBq. The BPW-34 photodiode was placed at the distance of 15cm from the source. During the 330 seconds of exposure we have registered 275 counts. This gives the detector sensitivity of $1.4 \cdot 10^6$ counts/R and efficiency $2.2 \cdot 10^4$. The later value is close to the calculated value $2.0 \cdot 10^4$.

As we consider the PIN photodiode as a replacement for Geiger-Müller tube we have to compare BPW-34 and tube with same size. Here we take for comparison the compact counter SBM-21 (see Table II).

Table II

Parameter:	BPW-34	SBM-21
Sensitivity for ^{137}Cs, counts/R	1.4	30
Operation voltage, V	30-40	260-320
Dimensions, mm	4.65×4.3×2	length: 21 diameter: 6

Although BPW-34 has lower sensitivity, due to small size one can create package from the several photodiodes to compensate this deficiency. Also it has lower operational voltage which is more suitable for practical applications.

For the spectrometry mode we have used ^{179}Ta and ^{241}Am sources. The measured spectra are shown in the Figs. 9 and 10.

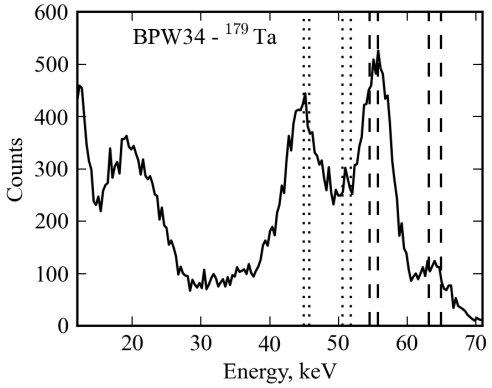

Fig. 9. Experimental energy spectrum for ^{179}Ta

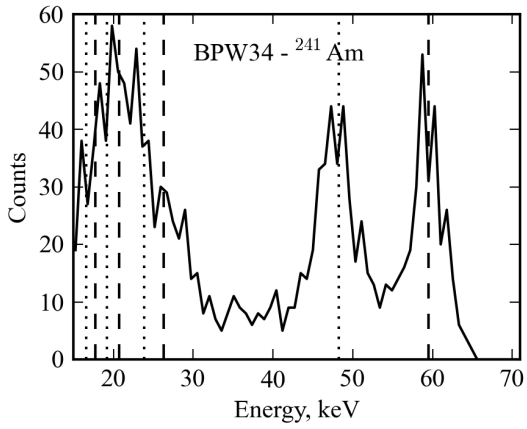

Fig. 10. Experimental energy spectrum for ^{241}Am

In the Figs. 9 and 10 dashed lines denote spectrum lines and dotted lines denote backscattering peaks (see Table I). According to the obtained spectra the backscattering intensity is comparable to the intensity of the primary radiation lines. This shows that detector module needs additional shielding to absorb the photons from Compton scattering on the surrounding construction elements.

Analysis of the experimental spectra gives the working parameters of the BPW-34 in spectrometry mode with the electronic circuit described in the Section II. The achieved characteristics are summarized in the Table III.

Table III

Operational energy range	15-60 keV
Energy resolution (FWHM) at 55.79 keV	6 keV (10%)
Noise level	6 keV

V. Conclusion

In the framework we have studied commercial PIN photodiode BPW-34 in counting and spectrometer mode. We have developed and tested low-noise electronic circuit with ADC and microcontroller capable to preprocess data from photodiode and to transmit it to computer.

Our theoretical calculations and experimental measurements actually show that PIN photodiodes are reliable alternative for compact Geiger-Müller tubes. This is valuable for practical purposes of development compact dosimetry devices for radiation monitoring, medical and industrial appliances.

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Mathematical Simulation of Conjugate Heat Transfer for Accumulator Batteries

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Abstract – **We consider mathematical simulation of conjugate heat transfer using finite elements method. Vehicle accumulator cooling system is studied and heat transfer is simulated using SolidWorks software. We have shown that air mixing in the air is efficient method to increase the heat transfer without additional air drag.**

I. Introduction

Modern environment-friendly electric powered and hybrid vehicles use lithium-ion batteries as power source. During operation such batteries produce a considerable amount of heat. This requires efficient cooling systems capable to provide steady temperature regime. At the same time vehicle appliances have weight and size restrictions, putting forward the demand on heat removal intensification for cooling systems. Numerical simulation is the efficient way to find the necessary technical solutions to optimize the parameters of vehicle cooling systems for further experimental research.

Thermal processes in the battery cooling systems are a case of conjugate heat transfer. The hydro- and thermodynamical characteristics of the system: the fields of temperature, velocity and pressure are determined by the coupled system of differential equations. This system of equations includes the heat transfer equation, describing the processes of heat transfer in a battery cell and a system of equations air flow hydrodynamics and the corresponding processes of forced convection. Analytical solution of the system for cases of practical interest is seldom possible, thus usually equations are sampled on a computational grid using the finite elements method [1]. Implementation of this method requires a solid model of the system, while development of the realistic solid model is a separate and rather challenging problem.

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Nowadays plenty of commercial software implements the finite elements method for heat transfer and fluid dynamics. In this paper we consider the simulation of heat transfer processes in the accumulator battery using SolidWorks 2011 (used to create a solid model) with SolidWorks Flow Simulation module. The later uses the finite volumes method for simulation of liquid flow and conjugate heat transfer.

II. Solid model of battery cells

Accumulator batteries for electric powered vehicles usually consist of a large number of individual power cells placed in a common housing. Simulation of the entire battery requires considerable computational resources; hence the detailed analysis of heat transfer processes becomes rather difficult. Within this paper we consider in detail heat transfer simulation for two adjacent power cells with air gap between them.

Firstly we consider the simple solid model for the single power cell. The solid model must reproduce the thermal properties of the real cell; in particular it should have anisotropic thermal conductivity [2]. Our model power cell is a solid box with geometrical dimensions of 150 × 200 × 12 mm. It has the longitudinal thermal conductivity 60 W/(m·K), lateral 1 W/(m·K) and specific heat of 0.8 kJ/kg. Each power cell is a 15 watts heat source.

Actually, our model contains two such cells with 3 mm air gap. To reduce the computational time we consider only the inner half volume of each power cell. This is possible due to symmetry properties of the simulating system.

The next are the boundary conditions. For the power cell we have adiabatic boundary conditions for outer surface $\partial\Omega_0$ and convective heat exchange for inner surface $\partial\Omega_1$:

$$\begin{aligned} (\vec{q}\vec{n})\big|_{\partial\Omega_0} &= 0 \\ (\vec{q}\vec{n})\big|_{\partial\Omega_1} &= h(T_s - T_{air}) \end{aligned} \qquad (1)$$

where $\vec{q} = -k\nabla T_s$ – heat flow in a power cell, k - thermal conductivity, $\vec{n}$ - the outer surface normal, h - the coefficient of convective heat transfer, T_{air} – the air temperature in the gap, T_s - the temperature of the power cell. Also both half volumes are uniform volumetric heat sources with heat power of 7.5 W each.

For air gap we have to specify both temperature and air flow boundary conditions:

$$\begin{cases} (\vec{v}_{air}\vec{n})\big|_{\partial\Omega_1} = 0 & T_{air}\big|_{\partial\Omega_{in}} = T_0 \\ (\vec{v}_{air}\vec{n})\big|_{\partial\Omega_{in}} = -v_0 & P_{air}\big|_{\partial\Omega_{out}} = P_0 \\ (\vec{q}\vec{n})\big|_{\partial\Omega_1} = h(T_{air} - T_s) \end{cases} \quad (2)$$

where T_0 and v_0 are inlet air temperature and velocity given on inlet $\partial\Omega_{in}$, P_0 - atmospheric pressure specified at the outlet $\partial\Omega_{out}$, and the heat flux is given on the inner surface, and outer are assumed to be adiabatic.

For calculations using SolidWorks Flow Simulation we also have to specify initial conditions even for the stationary problem. This is due to the fact that actually the calculation module solves the transient problem. The stationary solution is in fact the steady value of the corresponding calculated parameters.

III. Mathematical Simulation

The simple geometry described above is a reference point for further studies on heat transfer increase. The obvious way to do this - to increase the surface where the heat exchange occur through the installation of additional elements such as triangles, pins, etc. At the same time these additional elements increase air drag and the corresponding pressure drop. This, in turn, requires more powerful pumping facility, which degrades the performance of the real system cooling. Thus, the main task of the simulation is to optimize the geometry of the additional elements so that providing high heat transfer rate they still have relatively low air drag.

The cooling system for vehicle accumulator battery has certain limits on the air flow rates. High flow rates imply high performance pumping system and also lead to undesirable acoustic effects. Therefore for simulation we limit the range of air flow velocities to 1 - 4 m/s.

Fluid movement in the air gap is in general governed by Reynolds number

$$\mathrm{Re} = \frac{vd}{\nu}, \quad (3)$$

where v is fluid velocity, d is gap width and ν is kinematic viscosity. For our model the maximum air flow velocity is 4 m/s, gap width is 3 mm and hence the maximum Reynolds number is 700. The corresponding air flow is laminar. In this case installation of the additional elements in the gap does not lead to the onset of turbulence, even for sharp edges, steps, and similar elements. The only possible effects are higher convection rate due to overall surface increase and mixing of air flow due to these additional elements.

To analyze the effect of air flow mixing we consider the temperature profile in the air gap obtained from numerical simulations for the simple geometry. Figure 1 shows a typical temperature profile in the cross section of the air gap. It follows there is an overheated boundary layer, while central part of the airflow has lower temperature due to the low air thermal conductivity. This effect reduces the cooling efficiency for the case of simple geometry with smooth surfaces. In the case of cooling elements placed in the air gap the additional cooling effect could be achieved from the mixing of boundary and central parts of air flow.

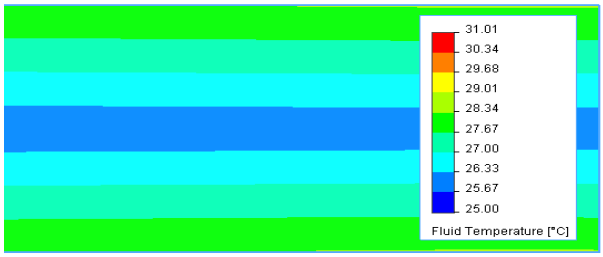

Fig. 1 Temperature distribution in the air gap

To analyze the contribution of convection and layer mixing to the heat transfer we perform simulation of cooling process with additional elements having zero thermal conductivity. In this case, increase the heat transfer takes place only due to the mixing of the air layers. Figure 2 shows comparison of calculated average surface temperature for cooling pins made from aluminum, the same pins made from thermal insulator and simple smooth surfaces. Obviously, there is no air mixing for the smooth surfaces – it is the reference point for comparison. From our simulation it follows that pins with zero thermal conductivity provide noticeable lower average surface temperature than smooth surfaces. This proofs that air mixing makes essential contribution to the heat exchange.

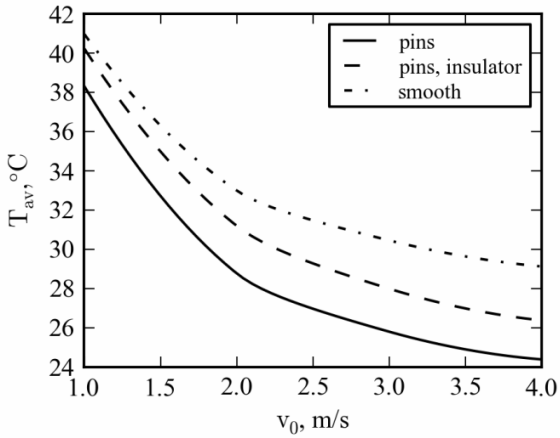

Fig 2. Comparison of average surface temperatures

It is possible to create cooling element that provides solely the airflow mixing. As such element we consider is twisted ribbon with twist pitch comparable to the width of the air gap. The ribbon width is slightly smaller than gap width. Figure 3 shows solid model that contains such elements. Cooling properties of such elements are insensitive to the ribbon material, as convection cooling in this case is negligible.

In order to compare the cooling efficiency we also developed the solid models with pins (Fig.4) and open pyramids (Fig.5) as cooling elements. The parameters of solid model are given in the Table I.

TABLE I

Model	**Twisted ribbons**
Width	3 mm
Thickness	0.2 mm
Twist step	10 mm
Row pitch	2.5 mm
Twist direction	alternating
Material	Aluminum
Model	**Pins**
Diameter	2.5 mm
Height	1.5 mm
Material	Aluminum
Row pitch	5 mm
Step	5 mm
Model	**Open pyramids**
Height	1 mm
Width	4 mm
Depth	2 mm
Vertex angle	60°
Row pitch	4 mm

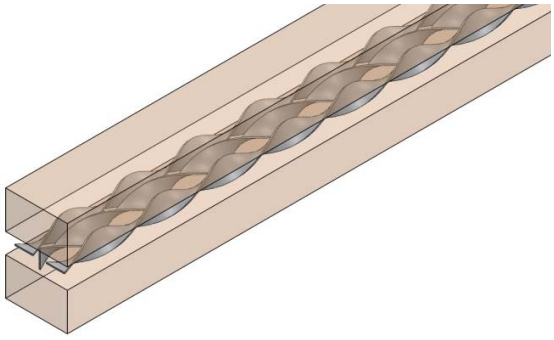

Fig. 3. Solid model of the power cell with twisted ribbons

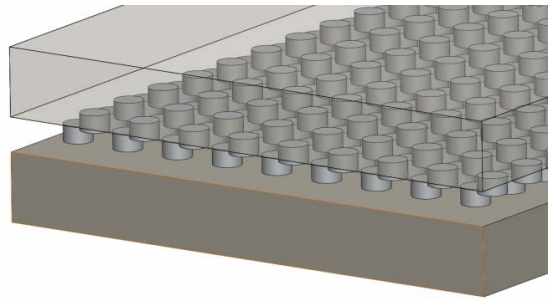

Fig. 4. Solid model of the power cell with pins

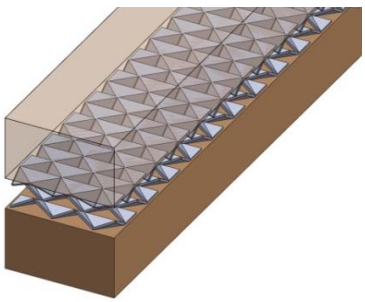

Fig. 5. Solid model of the power cell with open pyramids

IV. RESULTS AND DISCUSSIONS

We performed the detailed simulation of heat transfer processes using SolidWorks Flow Simulation. The main parameters that characterize cooling efficiency are average surface temperature of the power cell and pressure drop in the air gap. Another parameter that should be controlled is temperature drop along the power cell surface. For the real Li-Ion accumulator batteries this parameter should be less than 10ºC.

Figures 6 and 7 show the calculated surface temperatures and pressure drops in the air gap. As expected additional cooling elements increase heat transfer, but pressure drop in the air gap also increases. In all cases the temperature drop along the surface was within the 10□C limit.

From Fig. 6 one can see that for all cooling elements average surface temperature is almost the same and lower than for smooth surfaces. If we consider pressure drop we will find out that the twisted ribbon elements have the lowest (but still higher than for smooth surfaces).

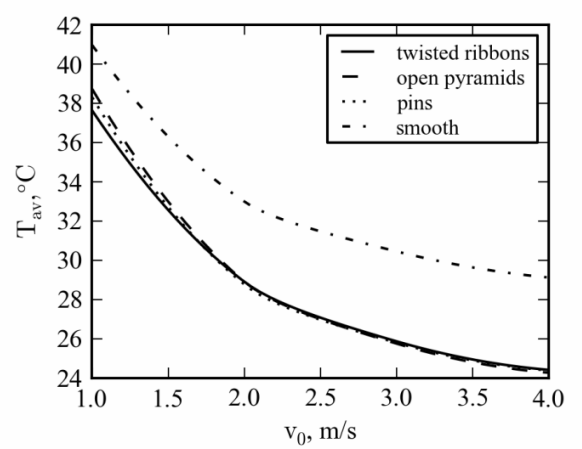

Fig 6. Average surface temperature for various surfaces

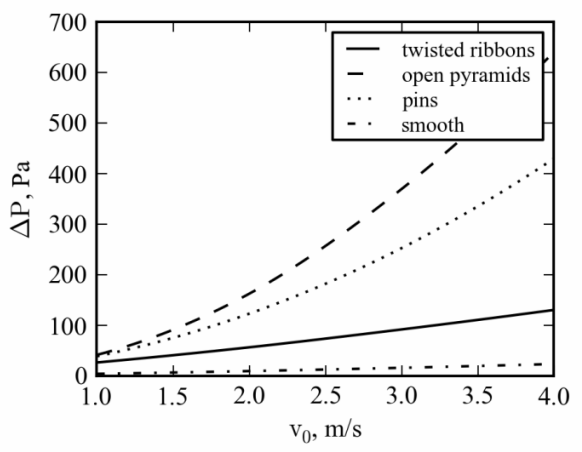

Fig 7. Pressure drop for various surfaces

The effect of twisted ribbons on the cooling airflow could be easily understood from figures 8 and 9. In the figure 9 the flow trajectories for twisted ribbons exhibit the high degree of rotation compared to essentially more straight

trajectories for pins (Fig 8.). This rotational movement causes the intensive air mixing and higher heat transfer from the power cell surface.

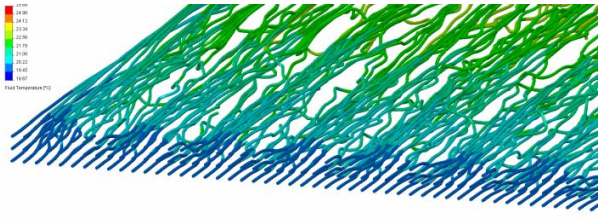

Fig. 8. Flow trajectories for pins

We performed the additional simulations to compare performance of twisted ribbons made from aluminum and thermal insulator. The both cases gave the similar results. This is additional proof that for twisted ribbons we have only intensive air mixing that leads to more efficient utilization of air heat capacity. From practical point of view this means that the different kinds of plastics and composite materials are suitable to manufacture these elements. This will reduce the overall weight of the battery compared to traditional metal cooling elements.

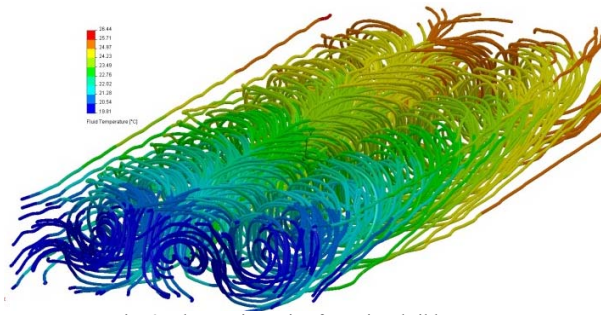

Fig. 9. Flow trajectories for twisted ribbons

V. Conclusion

The conclusions of the study reveal that cooling efficiency of the narrow air gap could be significantly increased by mixing of boundary and central parts of the air flow. Using mathematical simulation we have showed that this approach is more efficient than traditional methods utilizing pins or wing-like elements. These findings must be of considerable practical value for improving the cooling system design for electric vehicles accumulator batteries.

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Implementation of the Software for Research of Objects Detections of Passive Detectors of Movement

Lobur M. V., Holovatskyy R.I.

Abstract – **In this paper, by results of the lead probings a data domain, the software for research of objects detections of passive detectors of movement is offered. It is lead his successful embodying and testing. In the offered software singularities of a data storage of builders of model on a phisical layer in a DBMS have been considered. Data entry forms are developed and implemented. Export of a shaped database of standard signals to external files for data exchange with other software is stipulated.**

Keywords – **Implementation software, research the objects detection, passive motion detectors.**

I. Introduction

Owing to impetuous evolution of information technologies there are many software products which allow to lift on qualitatively new level scientific researches in various areas of a science and engineering [1-7]. To such software products should refer first of all: Axiom, Derive, Macsyma, Maple, MatLab, MathCAD, Mathematica, LabVIEW and many other things. Among all diversity of available software products is not present such which to the full would ensure needs of the scientist or the contributor. First of all it touches highly specialized researches. Such yields contain the powerful mathematical apparatus allowing to lead the most complicated evaluations but do not include a database in view of all necessary singularities proper in concrete researches [8]. One of such researches is the researches of objects detections of passive detectors of movement [9,10]. Therefore development infware and the software for researches of objects detections of passive detectors of movement in view of all delicacies of research experiment is actual.

II. Choice of method task. Select design environment

The researcher parameters of a desired signal which first of all interest will originate owing to occurrence in an area of detection of living plant. And the purpose of researches of objects detections of passive detectors of movement is determination of dependence of parameters of an output electric analog signal from variation of a thermal pattern in an area of detection. Therefore the developed system should contain: infological and datalogical database models, the block diagram of a database, structure of tables and connections between them. The system should ensure: simple inlet, renewal, variation of data necessary for the researcher and their machining; a lead-out of the gained outcomes in the necessary size; protection against unauthorized access and modification; the organization of an information accumulation from researchers; the convenient interface; possibility of interactive correction of the gated in data, preparation of reports by the gained outcomes of scientific researches for printing and a press on the printer or a plotter; visualization. Navigation of the necessary information by the given measure. Demands to system: a stable operation in a medium of Windows 9x/NT/2000/2003/XP/Vista/Windows7, at size from 32 MB of a RAM, on CPU starting from Intel of Pentium 133 MHz; convenience of operation of the user; orientation on a singularity of a data domain; reliability of system operation; protection against unauthorized interference; rationality of a data storage; protection against error conditions; the supervision of a regularity of data entry.

For embodying a task in view it has been sampled a medium of Microsoft Access, exterior SQL - server and Microsoft VisualBasic, as the programming language. Such choice motivated that in connection with intentions of our country to be integrated into the European Union and to adopt the civilized worth, including protection of intellectual property, even more often we collide with cases of check of the erected software on presence of the licence for it. In fact it is known, that to develop rigorous software products using such programming languages as C++, C#, Delphi, Java and others it is necessary to gain the licence which is not low-cost. The database is developed for researches of objects detections of passive detectors of movement is oriented in the core on its usage in scientific institutes, in particular at Lviv Polytechnic National University. In such establishments normally there are licences to use of the application package of Microsoft Office and accompanying programming language VisualBasic for Application.

Thus at start-up at once there is a main window of the program fig. 1.

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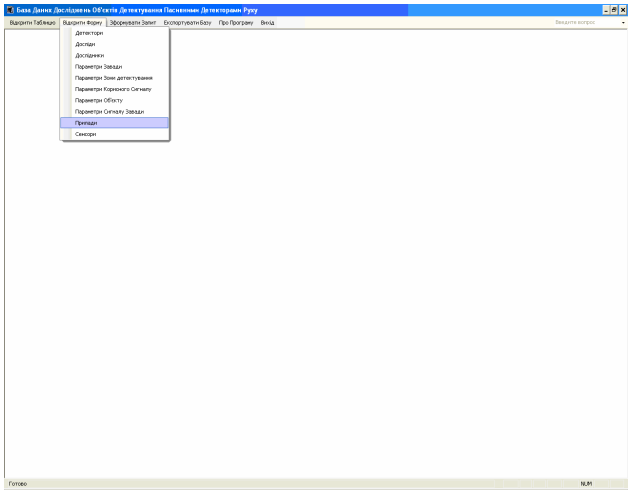

Fig. 1. The Main window of the program

As a result of a choice shown on a screenshot from above the menu will appear the shape " Devices" fig. 2.

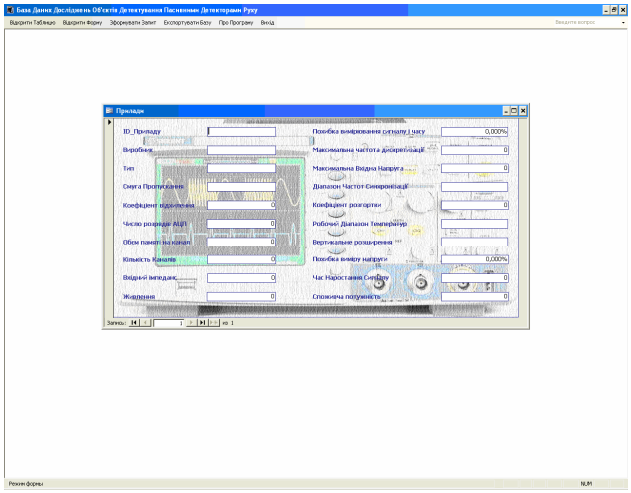

Fig. 2. A call of the menu of the shape " Devices"

III. DATA ENTRY FORMS

For the organization of the interface of the researcher with the developed database following shapes have been established: "Detectors", "sensor", "Options Zone detection", "researchers", "Options Signal Interference", "Interference Options", "Automatic", "experience", "Options useful signal", "Object Settings". By means of the developed shapes it is possible conveniently and to enter fast in a DB. Owing to that the shape allows to dispose data on the shield in the accidental order, data entry can be organized similarly to occupancy of the blank form, customary to the researcher, and also to apply some devices of automation of data entry. It is possible to realize survey and editing of data in a DB. The given shapes ensure a possibility of a lead-out to the shield of the information or her part in a condition sampled by the researcher. It simplifies modification, addings and removals of data from data base. By means of the developed shapes it is possible to retrieve data automatically from other linked tables; to perform computations under formulas; to hide or gate out some data depending on values of other fields. It is possible to use the developed shapes for control of a course of realization of the program. The important singularity of the developed shapes is control of a regularity of data entry that allows to reduce essentially quantity of errors arising on a stage of data entry.

The shape "Detectors" is showed on fig. 3.

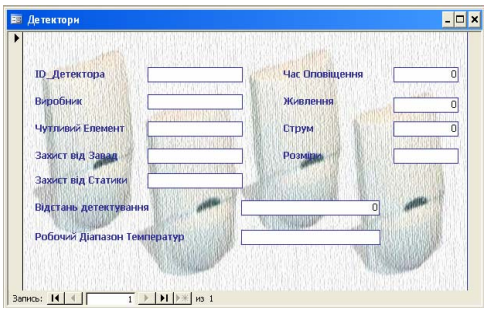

Fig. 3. The shape “ Detectors ”

The shape "Sensors " is showed on fig. 4.

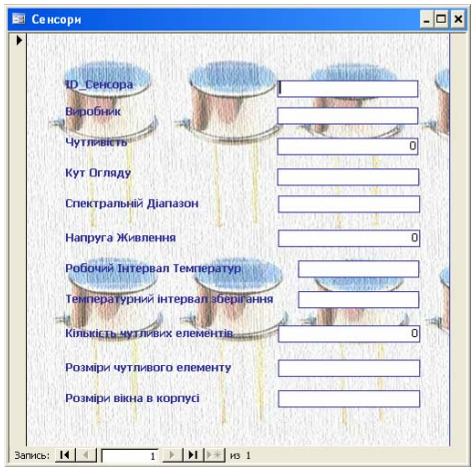

Fig. 4. The shape “Sensors”

The shape "Devices" is showed on fig. 5.

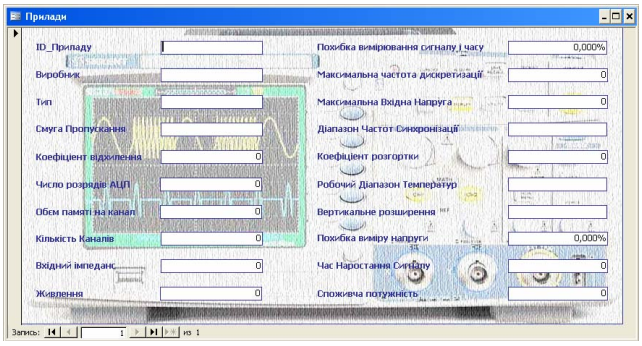

Fig. 5. The shape “Devices”

The shape "Researchers" is showed on fig. 6.

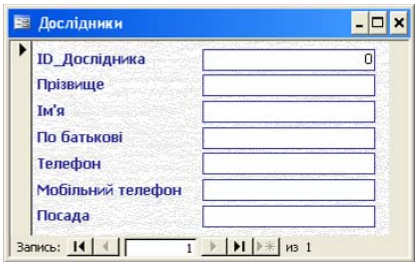

Fig. 6. The shape “Researchers”

The shape "Interference Options" is showed on fig. 7.

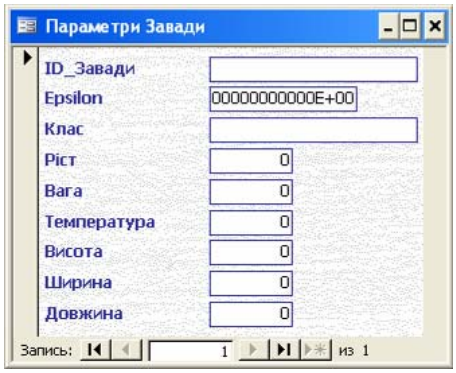

Fig. 7. The shape “Interference Options”

The shape "Experiments" is showed on fig. 8.

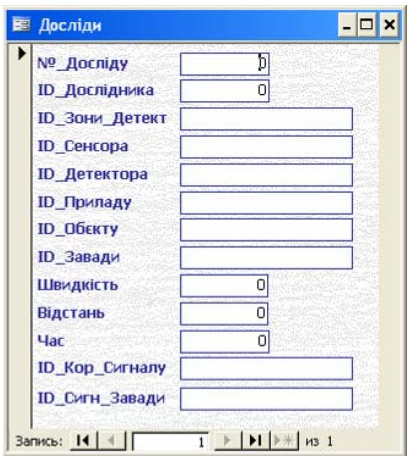

Fig. 8. The shape “Experiments”

The shape " Setup Zone Detection " is showed on fig. 9.

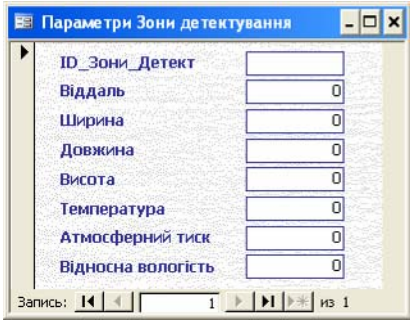

Fig. 9. The shape “Setup Zone Detection”

The shape " Parameters useful signal " is showed on fig. 10.

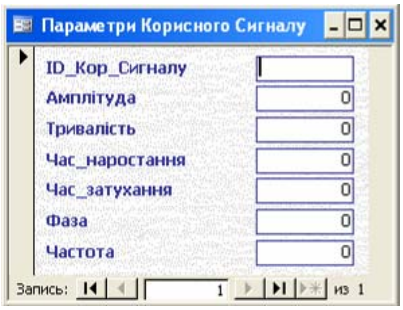

Fig. 10. The shape “Parameters useful signal”

The shape " Object Definitions " is showed on fig. 11.

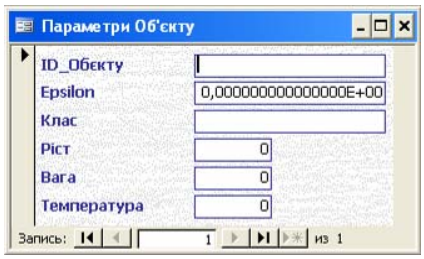

Fig. 11. The shape “Object Definitions”

The shape "The signal Interference" is showed on fig. 12.

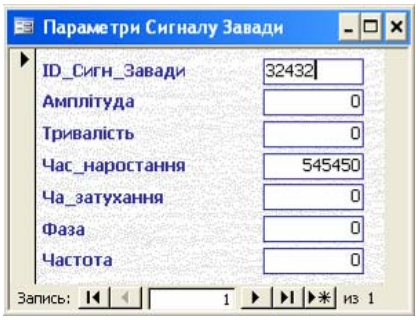

Fig. 12. The shape “The signal Interference”

Information about the program is called from the same choice and figured on fig. 13.

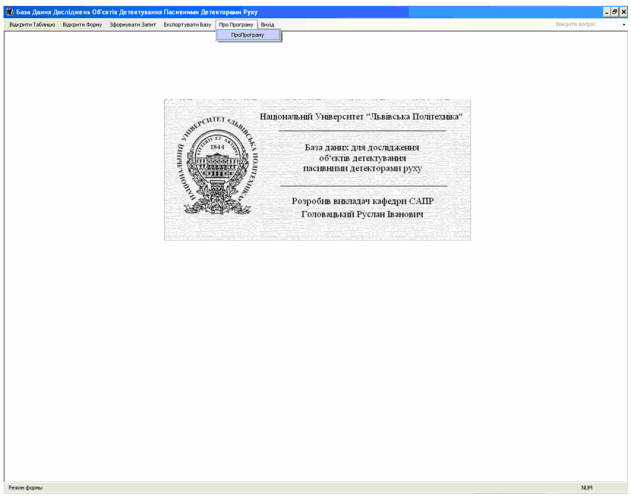

Fig. 13. A window of information about the program

IV. EXPORT OF THE FORMED DATABASE REFERENCE SIGNAL

As a result of scientific experiments gradually formed and filled with a database of useful reference signals and noise signals. This framework can be used to develop intelligent detectors solving the object recognition detecting passive motion detector. Therefore, this program provides the ability to export data to external files for further use, such as firmware in Flash Memory intelligent motion detector.

First, using SQL - queries on specific criteria formed a separate database of useful reference signal and reference signal noise. Example SQL - query database formation useful reference signals are shown in fig. 14.

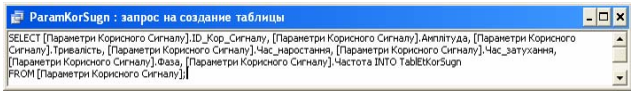

Fig. 14. SQL - query formation reference database of useful signals

Example SQL - the query form database reference signal noise is shown in Fig. 15.

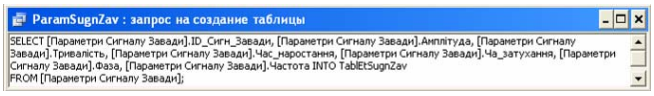

Fig. 15. SQL - query database formation reference signal noise

Then generated a database of reference signals can be stored in external files in fig. 16.

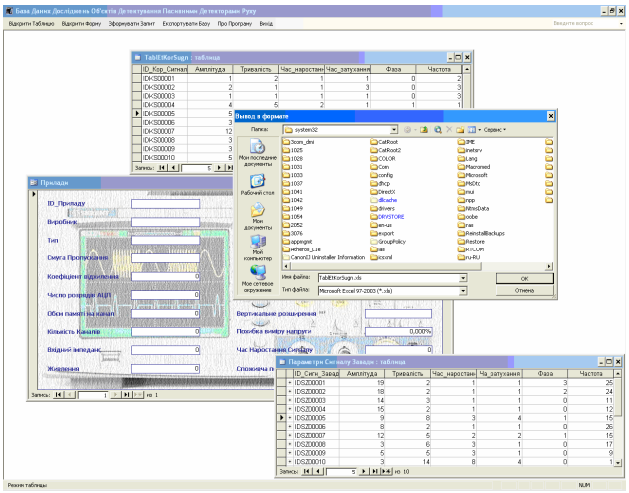

Fig. 16. Save a database of reference signals in external files

V. CONCLUSION

In this paper, by choice and justification of the method of software for research of objects detections of passive detectors of movement. Elected environment design. Given methodological support to work with the database. The problem of processing data in a scientific experiment to determine their structure and physical data representation formats. As a result of the research subject, based on the developed infological model, which could reflect this subject area as a set of information objects and their structural relationships have developed the software. With the developed infological model the next, datalogical, simulations have been described and taken into account properties of the concepts of the domain database objects detecting passive motion detector that was researches, the relationship and limits imposed on the data. Therefore, the actual software took into account the peculiarities of storage components model the physical layer in the database. Designed and implemented data entry forms. There exports formed the database of reference signals in external files for data exchange with other software. Thus developed, implemented and tested software for research of objects detections of passive detectors of movement.

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Mobile Technologies Based Distributed System for the Improvement of the Current Situation of Cyclists Moving within the Lodz Agglomeration

Krzysztof Strzecha, Tomasz Koszmider, and Konrad Stepien

***Abstract*— In this paper a distributed information system based on mobile technologies for the improvement of the current situation of cyclists moving within the Lodz agglomeration is described. The architecture of the system, its goals, research methodology and current state of work are presented.**

***Index Terms*— mobile technologies, iOS, Android OS, location services, GPS, map services, distributed systems, cycling, tourism.**

I. Introduction

In recent years, a bicycle is a popular means of transport, also among the inhabitants of Lodz agglomeration. Bike is increasingly becoming not only a great way to spend your free time, but also convenient and fast means of transportation within the city.

Unfortunately, Lodz agglomeration is not bicycle-friendly place. It is is one of the leaders in the ranking of the number of bicycle accidents in Poland [1]. In Lodz, and in other metropolitan cities, there are no reliable information solutions that help cyclists to find places that they should avoid and which can be dangerous for them.

There is no information about visiting the city on a bicycle. Bike trails are designated primarily outside the cities, so people using bikes for sightseeing purposes when coming to Lodz encounter difficulties moving between the places worth visiting.

New investments are often made without a reliable research about cycling in the city carried out, which makes them usually miss with real expectations and needs of cyclists.

Signing the Charter of Brussels, Lodz has committed (before 2020) to:

– increase to 15% of bicycles participation in city transportation;

– reduce by 50% the risk of bicycle accidents;

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– develop a system of bicycle parking facilities, and policies against theft of bicycles;

– increase the use of bicycles for commuting to school and work;

– promote the development of cycling tourism;

– cooperate with the cycling community, business and public institutions for popularization of cycling.

II. Project Description

In 2011, Computer Engineering Department of Technical University of Lodz in cooperation with InterData s.c. started work on a project sponsored by the Mayor of Lodz that can contribute to improving cycling in the urban area of Lodz by developing a distributed system based on mobile technologies. The finished system will allow:

– gathering information about bicycle traffic in the urban area of Lodz;

– analysis of collected data using specialized algorithms developed during the project;

– determination of optimal, safe cycling routes;

– integration with existing map services (i.e. Google Maps, OpenStreetMap).

– Data gathered during the project and results of its analysis should also enable:

– planning cycle investments according to the real needs of cyclists in Lodz;

– improving the safety of cycling in the urban area of Lodz;

– promoting the bicycle as a healthy, environmentally friendly and safe mode of transport;

– the development of cycling tourism in the Lodz agglomeration.

To the knowledge of the authors, the proposed research will be the first project of its kind in Poland. Existing solutions are based mostly on manual counting of cyclists, such as in Gdynia and Wroclaw, or on an automated counter of passing bicycles located under the road surface, as in Tychy. The main advantage of such solutions is their undoubted technological simplicity, but in contrast to the proposed solution, they do not allow to accumulate a lot of valuable data about bicycle traffic (e.g., the most frequently chosen routes, travel times, dangerous and friendly points).

III. The Research Methodology

Data collection for the project will be carried out in collaboration with the community of bikers through mobile devices equipped with GPS. The prevalence and wide availability of mobile phones with GPS and Internet access will enable low-cost acquisition of large amounts of data acquired during normal use of bicycles in everyday life.

A free application developed under the project, installed on a mobile device (phone, tablet) will automatically gathers information about the route that the cyclist is moving. Simple user interaction with the application will enable acquisition of additional data based on subjective assessment of the cyclist (places that are dangerous, friendly or interesting to cyclists). These data will be automatically sent to the server, stored in a database and analyzed. The processed results will be available to other users via mobile devices and desktop computers.

The essences of the project are to use inexpensive and widely available technology (mobile phones), to conduct the tests in the real environment and to give direct benefits to participants (access to the processed results). As a result, the cost of data acquisition will be limited to a minimum, and the data will be significantly consistent with the facts.

The acquired data will be analyzed using specialized algorithms developed during the project. Results of the analysis will enable design and implementation of changes in bicycle road infrastructure, determination of safe bicycle routes, their visualization and integration with mobile navigation systems.

IV. The Detailed Synopsis of the Project

The primary objective of the project is to improve the current situation of cyclists moving within the Lodz agglomeration by developing a distributed system based on mobile technologies (Fig. 1).

Within the project, it is necessary to complete the following tasks:

– development of the applications for mobile devices (phones, tablets) equipped with GPS technology;

– development of the server for the data recording and the results presentation;

– development of the data storage server;

– gathering data on cycling in the urban area of Lodz;

– development and implementation of the algorithms for the analysis of acquired data.

A. Application for mobile devices

Application for mobile devices will be developed in two versions for most popular hardware and software platforms of advanced mobile devices: Apple IOS [2] and Google Android [3].

The application will be automatically gathering information about the cyclist route. Simple user interaction with the application will enable acquisition of additional data based on subjective assessment of the cyclist (places that are dangerous, friendly or interesting to cyclists). In the user-selected time, collected data can be uploaded to the server at the center of the project. The application will also have the possibility to visualize the already processed data in order to use them by the rider while driving.

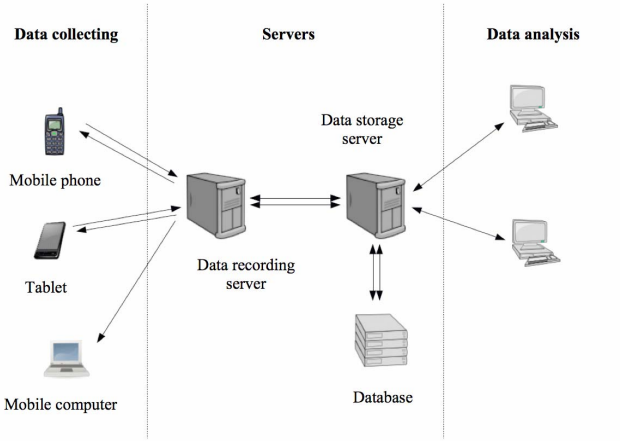

Fig. 1. Block diagram of the system, whose implementation is planned within the project

The application will be available free of charge to all cyclists who wish to contribute to increase the comfort and safety of cycling in the urban area of Lodz.

The use of cell phones as a tool for data collection will allow engagement of a large group of people without incurring additional costs.

B. Data recording server

The server for the data recording and the presentation of the results will be built as a WWW server. Transferring data and results will take place using standard HTTP requests. Access to research results will be possible not only by the application on the phone, but also through a standard web browser. The server will be integrated with existing map services (such as Google Maps, OpenStreetMap. In addition, the server will handle the project's website.

C. Data storage server

The data storage server will be the high performance relational database server. It will be intentionally separated from the data recording server, because the work related to the analysis of data can generate considerable load for the database and should not interfere with the functioning of the rest of the system.

D. Data collecting

The data necessary for the project will be collected using a free application developed for mobile phones. The authors predict that a large number of people, not directly related to the project, will be involved in this stage. People who use a bike as an everyday means of transportation or recreation will help to gather data that reflect the reality of cycling in the urban area of Lodz (routes with high intensity traffic, places generally regarded as safe or friendly for cyclists, etc.).

E. Data analysis algorithms

Within the project, specialized algorithms for analysis of bicycle traffic data will be designed for:

– development of maps of bike paths and cycling routes in the urban area of Lodz and its integration with existing map services (such as Google Maps, OpenStreetMap) and mobile navigation systems;

– planning of the changes in the road infrastructure on the basis of information about routes of special bicycle traffic and the cyclists dangerous and friendly places;

– automatic determination of bicycle routes between selected points in the Lodz agglomeration optimized in terms of comfort and security of transit;

– planning of cycling recreation and sightseeing, including locations of particular interest to the tourist and recreational points of view.

V. The Primary Effects of the Project

The direct result of the implementation of the project will be the development of an accurate map of the Lodz agglomeration showing traffic volume of cyclists in each location, and containing information on locations dangerous and friendly to cyclists.

The data collected and the results of their analysis can be used by the relevant departments in the cities of Lodz agglomeration to enhance the safety of cyclists by improving the existing infrastructure or introduction of appropriate information solutions. These data can also be an excellent source of information for planning future changes in the road infrastructure.

For cyclists measurable effect of the project will the ability to automatically determining the bicycle routes between selected points in the Lodz agglomeration optimized in terms of comfort and security of travel and the availability of tools to allow the planning of recreational cycling sightseeing including places of particular interest to the tourist and recreational points of view.

The authors hope that the solutions and tools worked out within the project will help in:

– the development of bicycle road infrastructure in the urban area of Lodz in accordance with real needs and expectations of cyclists;

– the improvement of safety and comfort of cycling in the urban area of Lodz;

– the effective promotion of the bicycle as a comfortable, fast and safe means of transport in Lodz, and thus increase the number of people ready to replace the existing means of transport (including car) on the bike, which in the long term can lead to a reduction in the number of cars in the city center (less pollution, less noise, safer cycling and walking);

– the effective promotion of cycling as a healthy, safe and interesting way of recreation and leisure activities by the inhabitants of Lodz agglomeration.

VI. The Evolution of the Project

During the work, the authors have decided to extend the scope of the merits of the project with additional forms of tourism and recreation, with particular emphasis on:

– hiking, both within the city (cultural tourism, entertainment, etc.) and out of the city (hiking tours),

– various forms of recreation, such as: jogging, nordic walking, skating, cross-country skiing.

Therefore, the additional result of the implementation of the project will be the development of an accurate map of the Lodz agglomeration showing the intensity of tourism and recreation in each location, and containing information on friendly and attractive places for tourists.

These data may also, in addition to the original version of the project, be used for:

– the designation of variety of themed walking trails within the city;

– the designation of new tourist trails and the detailed description of existing ones;

– the designation of specific routes for jogging, nordic walking, skating, cross-country skiing, etc.;

– the development of information solutions promoting various forms of tourism and recreation in the Lodz region.

The authors hope that the solutions and tools worked out within the project will help, in addition to the original version of the project, in:

– the development of infrastructure for hiking in the Lodz agglomeration in accordance with real needs and expectations of tourists;

– the effective promotion of hiking as a healthy, safe and interesting way of recreation and leisure activities by the inhabitants of Lodz agglomeration;

– the development of infrastructure for the active forms of recreation (e.g., jogging, nordic walking, skating, cross country skiing, etc.) in the Lodz agglomeration in accordance with real needs and wishes of the people;

– the effective promotion of active forms of recreation (e.g., jogging, nordic walking, skating, cross country skiing, etc.), as a healthy, safe and interesting way of recreation and leisure activities by the inhabitants of Lodz agglomeration;

– the development of tourism infrastructure in the city (walking routes, help desks, etc.);

– the effective promotion of Lodz agglomeration, as a friendly and interesting place for visitors who prefer various forms of tourism and recreation;

– the effective promotion of existing and creation of new potentially attractive places from a tourist point of view (museums, cinemas, theaters, monuments, restaurants, cafes, taxi stops, public transportation, etc.);

– the increase of the tourist attractiveness of Lodz agglomeration.

It should be noted that solutions worked out within the project could contribute to the development of other forms of tourism at the urban area of Lodz, not directly included to the content of the project. For example, the development

of walking trails and information solutions on tourist attractions may contribute to an increased interest in Lodz and the surrounding area as center for conference and trade tourism.

VII. The Current State of the Project

During the work on the project, a series of tasks was already completed. Authors have decided to present the most significant ones in terms of project success.

The data on existing communications infrastructure, with particular emphasis on cycling and walking tours (bike paths, hiking trails) and the attractions and places for recreation was collected.

The beta version of the application for mobile devices running the Android OS and Apple iOS was designed and implemented (Fig. 2). The application is in the process of extensive testing using a variety of mobile devices (phones, tablets).

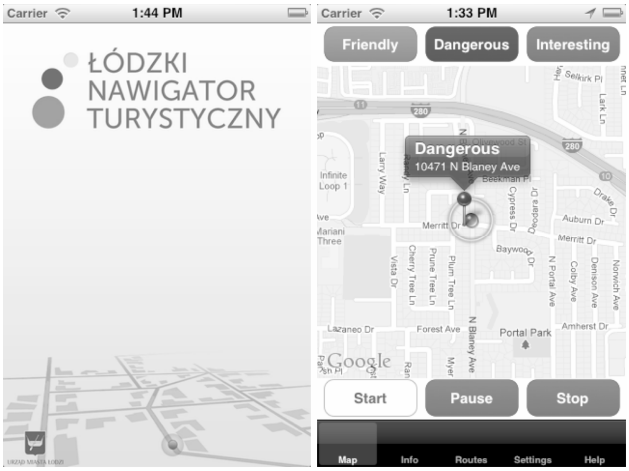

Fig. 2. Beta version of application developed for iOS mobile devices running under control of iPhone simulator

Installation and configuration of server's software was carried out. CentOS Linux was used as a operating system, MySQL as a database and Apache/PHP as a web-based environment. CentOS Linux combines the flexibility of a Linux distribution with enterprise-class reliability. Selection of server software (Apache, PHP, MySQL), was mainly due to the fact that these programs are well known, well documented and very stable in operation.

Mobile devices transmit the collected data as a SQLite database files. The transmission takes place using HTTP POST. Using SQLite format greatly simplified the implementation, since it is a format supported by both mobile systems and server platform.

Once a day, the newly uploaded files are converted to a MySQL database and sent to the server storing the data. This solution allows performing complex data processing operations on the storage server without visible effects on the functioning of the system (users only use the data recording server).

Preliminary work was performed on the integration of the system being developed with web map services: Google Maps, OpenStreetMap, OpenCycleMap.

The website promoting the project was prepared. In the construction of website a content management system WordPress was used. This solution provides a simple service management, updating and further development. Website promoting the project is available at: http://lodzkinawigatorturystyczny.dot.pl/.

VIII. Conclusion

In this paper the mobile technologies based distributed system for the improvement of the current situation of cyclists moving within the Lodz agglomeration was presented. When finished, system may contribute to significant improvements in safety and comfort of cyclists within the Lodz agglomeration and, consequently, to popularize cycling as an everyday means of transportation and recreation. In its expanded form, system should help to increase the tourist attractiveness of Lodz and the surrounding area.

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Extrema Envelope Function Multibeam Interference Fabry-Perot. Part I. Properties and Applied Aspects for Plane-Parallel Single-Layer Systems

P. S. Kosoboutskyy, M. S. Karkulovska

***Abstract*— In the first part of the work the regularities of the envelope functions of the amplitude-phase spectra of the Fabry-Perot multiple-beam interference for electromagnetic are generalized. Basic physical principles extending the possibilities of the envelope function method for the determination of structure parameters for the single layer are formulated.**

***Index Terms*— antireflection, Fabry-Perot interference, envelope function.**

I. Introduction

IT is known that by itself the problem of Fabry-Perot interference was formulated and began to be theoretically studied long ago [1]-[2]. The recurrence formulas for the analysis of reflecance and transmittance curves in the interference extrema were found on the basis of taking into account multiple reflections of beams in films with the subsequent coherent combination by Vlasov [3], and later Lisitsia [4] obtained concrete expressions for reflectance of a plane wave by a system by plane parallel interfaces.

An important aspect in the interference approach to the research of reflection and transmission properties of film surfaces is the analysis in the area of the Fabry-Perot interference extrema formation, on the basis of which the method of the envelopes of their intensity has been developed. In the case of a single-film, for the particular models of reflection an obvious type of the analytical expressions of the envelope function at normal reflection was found in the works [5]-[9] and only recently [10], [11] this method has been generalized for the arbitrary geometry of experiment, ***s***- and ***p***- polarized wave, and arbitrary level of absorption, and for extrema ellipsometry spectra [12] – [14].

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Taking into account a wide range of practical applications of systems with multiple-beam coherent signal combining in optical filters [15], sensors [16], [17], the properties of the envelopes of the FPIE are generalized in the first part of this paper on the basis of the results of the original research, hence the physical principles of the diagnosis of single-layer coating parameters have been formulated.

II. Model, Main Relations and Basic Conclusions

Let the plane light wave of arbitrary ***s***- and ***p***-polarization propagate in the semi-infinite medium (index 0) with refractive index n_0 and fall at an arbitrary incidence angle α on the surface of a layer (index 1). The layer have a geometrical thickness d, complex a refractive index $\tilde{n}_1 = n_1 - i\chi_1$, in which a wave undergoes a complex phase shift $\tilde{\delta} = \frac{4\pi d}{\lambda}\tilde{n}_1 \cos\tilde{\beta}$, where $\tilde{\beta}$ is a complex angle of refraction on the ambient-layer interface.

It is known that for single interfaces the amplitudes of complex coefficients of reflection $\tilde{r} = \sigma\exp(-i\phi)$ and transmission $\tilde{t} = \tau\exp(-i\varphi)$ at an arbitrary angle of light incidence for both ***s***- and ***p***-polarization are determined by the known formulas

$$\tilde{r} = \frac{\tilde{r}_{01} + \tilde{r}_{12}\Omega\exp(-i\delta)}{1 + \tilde{r}_{01}\tilde{r}_{12}\Omega\exp(-i\delta)}, \tilde{t} = \frac{\tilde{t}_{01}\tilde{t}_{12}\sqrt{\Omega}\exp\left(-i\frac{\delta}{2}\right)}{1 + \tilde{r}_{01}\tilde{r}_{12}\Omega\exp(-i\delta)} \quad (1)$$

where $\Omega = \exp\left(\mathrm{Im}\,\tilde{\delta}\right)$, $\delta = \mathrm{Re}\,\tilde{\delta}$, $\tilde{r}_{01,12}$ and $\tilde{t}_{01,12}$ are wellknown Fresnel amplitude coefficient for each single intrerface, ϕ and φ are the respective phase shifts. The resonant complex coefficients of reflection and transmission for both polarizations are modeled by the Lorentz single-oscillator function

$$\tilde{\varepsilon}(\omega) = \varepsilon_0 + \frac{4\pi\lambda\omega_0^2}{\omega_0^2 - \omega^2 - i\omega\gamma}, \quad (2)$$

where ε_0 is the background dielectric constant at low frequencies; $4\pi\lambda$ is the oscillator force on the resonant frequency ω_0; γ is the damping parameter.

According to (1) the energy coefficient of reflection R and transmission T, and the tangent of phases $\tan\phi$ of wave are defined as follows

$$R = \frac{\sigma_{01}^2 + \Theta^2 + 2\sigma_{01}\Theta\cos 2\Delta^-}{1 + \sigma_{01}^2\Theta^2 + 2\sigma_{01}\Theta\cos 2\Delta^+},$$
$$T = \frac{n_2\cos\gamma}{n_0\cos\alpha}\frac{T_{01}T_{12}\Omega}{1 + \sigma_{01}^2\Theta^2 + 2\sigma_{01}\Theta\cos 2\Delta^+} \quad (3)$$

and

$$\tan\phi = \frac{\mathrm{Im}\,\tilde{r}}{\mathrm{Re}\,\tilde{r}} = \frac{\sigma_{01}\left(1-\Theta^2\right)\sin\phi_{01} + \Theta\left(1-\sigma_{01}^2\right)\sin\left(\phi_{12}-\delta\right)}{\sigma_{01}\left(1+\Theta^2\right)\cos\phi_{01} + \Theta\left(1+\sigma_{01}^2\right)\cos\left(\phi_{12}-\delta\right)} \quad (4)$$

where $T_{01,12} = \tilde{t}_{01,12}\cdot\tilde{t}^{*}_{01,12}$, $\Theta = \sigma_{12}\Omega$, $\Delta^{\pm} = \frac{\delta \pm \phi_{01} - \phi_{12}}{2}$. Then expression for energetic coefficients reflection and transmission are defined as [7]:

$$R = \frac{R_m + b^2\cos^2\Delta^-}{1 + b^2\cos^2\Delta^+} = \frac{R_M - a^2\sin^2\Delta^-}{1 - a_1^2\sin^2\Delta^+},$$
$$T = \frac{T_m}{1 - a^2\sin^2\Delta^+} = \frac{T_M}{1 + b^2\cos^2\Delta^+}, \quad (5)$$

where the values of these power coefficients in the extrema $R_{m,M}$ and $T_{m,M}$ (m is the index of the minimum extrema, and M is the index of the maximum extrema), $a^2 = \frac{4\sigma_{01}\Theta}{\left(1+\sigma_{01}\Theta\right)^2}$, $b^2 = \frac{4\sigma_{01}\Theta}{\left(1-\sigma_{01}\Theta\right)^2}$. Here the angle of incidence α, angle of refraction β at the boundary 12 and angle of refraction γ at the boundary 23 are related by known Snell`s law $n_0\sin\alpha = n_1\sin\beta = n_2\sin\gamma$. For the phase spectra the analytical form of envelope expression could be determined only for the reflected wave as:

$$\phi_{M,m} \cong 2\pi \pm \frac{\sigma_{01}\left(1-\sigma_{12}\Theta\right)\sin\phi_{01} + \sigma_{12}(1-\sigma_{01}^2)\Omega}{\sigma_{01}\left(1+\Theta^2\right)\cos\phi_{01}}, \quad (6)$$

which under the condition $\phi_{01,12} \cong m\pi$ is simplified to the form $\phi_{M,m} \approx 2\pi \pm \frac{(1-\sigma_{01}^2)\Theta}{\sigma_{01}(1+\Theta^2)}$.

The essence of the most important regularities of envelopes (5) and (6) consists in the following.

1. Functions (5) and (6) are the general analytical expressions of FPIE envelopes of multibeam interference of electromagnetic plane and gaussian beam light of ***s***- and ***p***-polarized waves; they are valid for both transparent and absorbing structures at the normal and oblique incidence of light. The phase spectra are described correctly by the envelope method only in the reflection geometry.

2. The points of contact of envelope functions with the Fabry-Perot contours on the side of the maxima $R = R_M$ and minima $R = R_m$ are determined by the following conditions

$$a^2 = 0, \quad \sin^2\Delta^{\pm} \neq 0, \quad (a)$$
$$a^2 \neq 0, \quad \sin^2\Delta^{\pm} = 0, \quad (b)$$
$$b^2 = 0, \quad \cos^2\Delta^{\pm} \neq 0, \quad (c)$$
$$b^2 \neq 0, \quad \cos^2\Delta^{\pm} = 0, \quad (d) \quad (7)$$

and they do not necessarily have to be the points of the extrema. Conditions (a) and (c) correspond to the manifestations of Brewster effect (pseudo-effect) on the opposite single interfaces, and (b) and (d) correspond to phase compensations in the points of contact with the envelope functions of the maxima $\Delta_1 = m\pi$ (7b) and minima $\Delta_1 = \left(m + \frac{1}{2}\right)\pi$ (7d) in multiple-beam interference [23].

3. 2π periodicity of the Fabry-Perot spectra makes it possible to define an area under the contour of an arbitrary maximum, excluding the area under the envelope of the minima, as

$$S_M = \frac{1}{2\pi}\int_0^{2\pi}(R - R_m)d\delta. \quad (8)$$

Within the limits of one extrema the integral (8) has the form $S_M = \frac{1-R_m}{2\pi}\left[\int_0^{2\pi} d\delta - \int_0^{2\pi}\frac{d\delta}{1 + b^2\cos^2\frac{\delta}{2}}\right]$ and equals

$$S_M = \left(1-R_m\right)\left[1 - \frac{1}{\sqrt{1+b^2}}\right]. \quad (9)$$

Assuming that within the limits of the 2π–band of the interference the parameters $\phi_{01,12}$, b, R_m change insignificantly and replacing the value of the power reflection coefficients R_m in the nearby minima with an average value we will find that the expression for an area under the contour of reflection is simplified to the form

$S_M \approx R_M\left[1-\frac{1}{\sqrt{1+b^2}}\right]$. In the area of a single oscillator resonance transition (2), the functions $\Delta^{\pm}$ have synchronous oscillations, therefore the area limited by the maximum of reflection will equal

$$S_M = 2\pi\frac{2\sigma_{01}\sigma_{12}\left(1-\sigma_{01}^2\right)\left(1-\Theta^2\right)}{\left(1+\sigma_{01}\Theta\right)\left(1-\Theta\right)^2}\Omega \qquad (10)$$

and shows dependent of the about frequency and absorption level of the wave in the layer [20].

4. The envelope contour for a single layer does not oscillate, so far as Fabry-Perot extrema limit the width of the amplitude-phase spectra oscillations as the width of the layer varies. The differences of envelopes $\Delta R = R_M - R_m$ and $\Delta T = T_M - T_m$

$$\Delta R = 2\Theta\frac{1-\sigma_{01}^2}{1-\sigma_{01}^2\Theta^2}$$
$$\Delta T = \frac{\cos\gamma}{\cos\alpha}\frac{n_2}{n_0}\frac{T_{01}T_{12}\Omega}{\left(1\mp\sigma_{01}\Theta\right)^2}\frac{4\sigma_{01}\Theta}{\left(1-\sigma_{01}^2\Theta^2\right)^2} \qquad (11)$$

determine the ranges of the energy coefficients that correspond to the changes in geometrical layer thickness, under condition of invariable optical parameters of the media. As it is shown in Fig.1, there occur at the frequency ω_i the points of dielectric contrast disappearance between the film and substrate (isotropic point [21]) where Fabry-Perot oscillations will collapse out and $\Delta R = 0$, $\Delta T = 0$, $\Theta = 0$, and envelopes $R_M = R_m$, $T_M = T_m$ will contact each other. At the isotropic point the Fabry-Perot contours will invert.

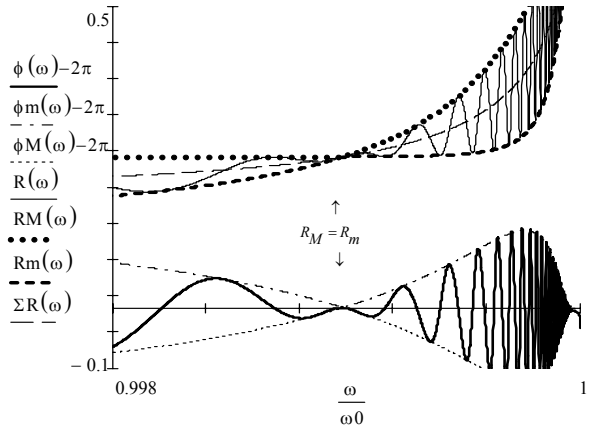

Fig. 1

In the interval the frequency $\omega < \omega_0$, provided that for optical parameters of layer $n_1 \rangle\rangle \chi_1$, and $\mathrm{Re}\,\tilde{\varepsilon} \rangle\rangle \mathrm{Im}\,\tilde{\varepsilon}$, then from equations $n_{0,2}^2 \cong n_1^2(\omega_{i01,12})$ for following analytical expression for the frequency ω_i are obtained:

$$\omega_{i,01,12} \cong \omega_0\sqrt{1\pm\frac{4\pi\chi_1}{\varepsilon_0 - n_{0,2}^2}}, \qquad (12)$$
$$"+" - \varepsilon_0 \rangle n_{0,2}^2; \quad "-" - \varepsilon_0 \langle n_{0,2}^2$$

At the frequency ω_i for each interface the energetic coefficient $R_{\omega_{i01}} = \sigma_{12}^2$ and $R_{\omega_{i12}} = \sigma_{01}^2$ from

$$\sqrt{R_{m,\omega_{i01}}} = \begin{cases}\frac{n_0 - n_1}{n_0 + n_1}, & n_0 \rangle n_1,\\ \frac{n_1 - n_0}{n_1 + n_0}, & n_0 \langle n_1.\end{cases}$$

$$\sqrt{R_{m,\omega_{i12}}} = \begin{cases}\frac{n_1 - n_2}{n_1 + n_2}, & n_1 \rangle n_2,\\ \frac{n_2 - n_1}{n_2 + n_1}, & n_2 \langle n_1.\end{cases}$$

5. The quadratic form of the envelope functions (5) makes it possible to redefine the visibility of the extrema as [22]:

$$W_{R,T} = \frac{\sqrt{(R,T)_M} - \sqrt{(R,T)_m}}{\sqrt{(R,T)_M} + \sqrt{(R,T)_m}}. \qquad (13)$$

In contrast to the approach adopted according to Michelson [23], the approach (13) substantially simplifies the analytical expressions for visibility:

$$W_R = \frac{\left(1-\sigma_{01}^2\right)\Theta}{\sigma_{01}\left(1-\Theta^2\right)}, \qquad W_T = 2\sigma_{01}\Theta. \qquad (14)$$

Taking into consideration the condition of experimental observation of the extrema $\Theta^2 << 1$, the logarithmic dependences on the frequencies scale are equal to

$$\ln W_R \cong \ln\left[\frac{\sigma_{12}}{\sigma_{01}}\left(1-\sigma_{01}^2\right)\right] + \frac{4\pi d}{\lambda}\chi_1 \qquad (15)$$
$$\ln W_T \cong \ln(2\sigma_{01}\sigma_{12}) + \mathrm{Im}\,\tilde{\delta}$$

i.e. they become practically linear, and in the region of the constancy of the absorption level in the layer $\chi_1 \cong const$ the slopes $\ln W_{R,T}$ coordinate with the slope $\mathrm{Im}\,\tilde{\delta}$ to the constant. The lineare type of the dependence of (15) makes it possible to determine the absorbing coefficient χ_1 as $\chi_1 \cong \frac{\lambda}{4\pi d}\ln\left[W_R\frac{\sigma_{01}}{\sigma_{12}}\right]$. Here the connection between the visibilities $W_{R,T}$ and according to Michelson $V_{R,T}$ is established by means of the transformation

$$2\frac{x+y}{x-y} = \frac{\sqrt{x}+\sqrt{y}}{\sqrt{x}-\sqrt{y}} + \frac{\sqrt{x}-\sqrt{y}}{\sqrt{x}+\sqrt{y}},$$

whence $V_{R,T} = 2\left[W_{R,T}^{-1} + W_{R,T}\right]^{-1}$.

6. Within the limits of the 2π–band the following equality holds: $\frac{R_M - R}{R - R_m} = \frac{T - T_m}{T_M - T} = \left(\frac{a}{b}\right)^2 \tan^2 \frac{\Delta^{+,-}}{2}$. Its left parts change in the scope $[0,+\infty]$ and on the Fabry-Perot contour on both sides in relation to the points of the maximum it is always possible to single out the frequencies ω_Σ and $\omega_\Sigma + \Delta\omega_\Sigma$, which correspond to the phase thicknesses δ_Σ and $\delta_\Sigma + \Delta\delta_\Sigma$, for which the following relations hold: $\frac{R_M - R}{R - R_m} = \frac{T - T_m}{T_M - T} = 1$. On these frequencies the power coefficients are equal to

$$\Sigma_{R,T} = \frac{1}{2}\left[(T,R)_M + (R,T)_m\right]. \qquad (16)$$

As shown in fig.1, the contours $\Sigma_{R,T}$ (16) do not oscillate and for them the (16) hold, for which multiple-beam interference disappears. The spectral width of the interference bands $\Delta\omega_\Sigma$ at (16) level is related to the remains above the 2π of the wave phase shift $\Delta\delta_\Sigma$ by means of the expression

$$\Delta\delta_\Sigma = \frac{\pi}{2}\frac{\Delta\omega_\Sigma}{\Delta\omega_{mM}}, \qquad (17)$$

where $\Delta\omega_{mM} = \omega_m - \omega_M$ is the spectral resolution between the adjacent minimum and maximum. Since the values $\Delta\omega_{mM}$ and $\Delta\omega_\Sigma$ included in (17) are experimentally determinable, it is possible to estimate the remains of the phase thickness $\Delta\delta_\Sigma$ in relation to the phase period 2π.

7. In an arbitrary geometry and polarization of a wave, the experimentally determined values of the power coefficients $(R,T)_{M,m}$ and the structure parameters σ_{01}, σ_{12}, Ω_1 are connected by means of a system of equations

$$\sigma_{01} = \Psi \pm \sqrt{1+\Psi^2}, \quad \Theta = \frac{\sigma_{12} - \sqrt{R_M}}{\sigma_{12}\sqrt{R_m} - 1}, \qquad \sigma_{01}\Theta = \frac{\sqrt{T_M} - \sqrt{T_m}}{\sqrt{T_M} + \sqrt{T_m}} \qquad (18)$$

making it possible to determine the optical characteristics of the system where $\Psi = \frac{1 + \sqrt{R_M R_m}}{\sqrt{R_M} + \sqrt{R_m}}$. The system of equations is applicable to an arbitrary geometry of experiment and light polarization.

8. The method of envelope functions is effective in the area of resonance dispersion of the substrate for the determination of the phase layer thickness of the nanoscale $\delta << 2\pi$. In the point of contact of the envelope function of the minima with the reflection contour $R = R_m$ the condition of the phase compensation [19], [24] holds and it is localized on the frequency

$$\omega_m = \omega_0\sqrt{P_1 + \sqrt{P_1^2 - P_2}}, \qquad (19)$$

where

$$P_1 = 1 + \frac{4\pi\hat{\chi}}{\varepsilon_0} + \left(\frac{\gamma}{\sqrt{2}\omega_0 \tan\delta}\right)^2, \; P_2 = 1 + \left(\frac{4\pi\hat{\chi}}{\varepsilon_0}\sin\delta\right)^2.$$

It is noted here that on the frequency ω_m the tangent of the phase thickness of a layer is $\tan\delta = \tan\phi_{12}$. Therefore, the equality

$$\varepsilon_0^2 + \varepsilon_1^2 + \varepsilon_2^2 + 2\varepsilon_0\varepsilon_2 ctg^2\delta = \frac{2\varepsilon_0}{\sin^2\delta}\sqrt{\varepsilon_1^2 + \varepsilon_2^2}$$

holds and the dispersion equation takes the form

$$n_2^4 + \varepsilon_0^2 + 2\varepsilon_0 n_2^2 ctg^2\delta + \frac{4\pi\hat{\chi}\omega_0^2\left[4\pi\hat{\chi}\omega_0^2 + 2\left(\omega_0^2 - \omega^2\right)\left(n_2^2 + \varepsilon_0 ctg^2\delta\right)\right]}{(\omega_0^2 - \omega^2)^2 + \omega^2\tau^2} =$$

$$= \frac{2n_1^2}{\sin^2\delta}\sqrt{\varepsilon_0^2 + \frac{4\pi\hat{\chi}\omega_0^2\left(4\pi\hat{\chi}\omega_0^2 + 2\varepsilon_0\left(\omega_0^2 - \omega^2\right)\right)}{(\omega_0^2 - \omega^2)^2 + \omega^2\gamma^2}},$$

where $\tilde{\varepsilon} = \varepsilon_1 + i\varepsilon_2$. In the limit of $\gamma \langle\langle \omega_0$ we obtain that

$$\left(\frac{\omega_m}{\omega_0}\right)^2 \approx 1 + \frac{4\pi\hat{\chi}}{\varepsilon_0}\cos^2\frac{\delta}{2}. \qquad (20)$$

Hence, if the phase thickness of the layer is $\delta = 2\pi, 4\pi....$, the frequency ω_m is localized in the vicinity of ω_L ($\omega_m \to \omega_L$), where ω_L is the longitudinal frequency. For $\delta = \pi, 3\pi, 5\pi...$, the minima is localized at the frequency ω_0 ($\omega_m \to \omega_0$). Therefore, a change in the phase thickness of the layer to a periodic variation of frequency of the minima of contour reflection ω_m within the limits of the longitudinal-transverse splitting $\Delta\omega_{0L} = \omega_L - \omega_0$ as shown on the Fig. 2.

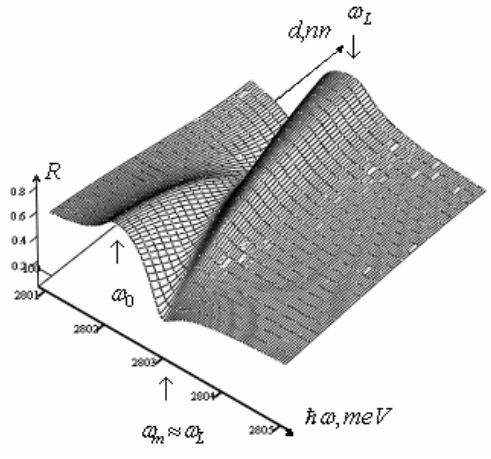

Fig. 2

In the case of the vanishing layer thickness $\delta \to 0$ the expression (20) coincides with the known Lyddane-Sachs-Teller relation $\omega_m = \omega_0 \sqrt{1 + \frac{4\pi\alpha}{\varepsilon_0}}$ [25].

III. Conclusion

1. Theoretical investigation of of the spectral characteristics of the envelopes of reflection and transmission spectra of light by single-layers strusture has been carried out. The general the analytical expressions for the envelopes of transparent and absorbing structures at the normal and oblique incidence of plane electromagnetic and acoustic wave of both polarization (s and p) are found. It is shown, that the envelope function can be connected between extremum reflecting and transmitting energetic coefficients and parameters of layers.

2. In the single-film coatings the envelopes of Fabry-Perot spectra intercept at the expense of spectral dispersion of refraction index one of the media which form plane-parallel film.

3. The main conclusions about the envelopes of the Fabry-Perot extrema for single-layer coatings we should note that the above-mentioned conclusions are also valid for Gaussian beams, within the validation of the Fabry-Perot principle for them.

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On Graph-Based Image Segmentation Using Graph Cuts in Feature Space

Anna Fabijańska

***Abstract*—In this paper problem of graph based image segmentation is considered. Modification of min-cut/max-flow algorithm is proposed. The main change introduced by the proposed approach is to regard neighborhood in feature space rather than spatial neighborhood of pixels as in case the original method. Results provided by the proposed approach are presented, compared with the results of the source method and discussed.**

***Index Terms*—Image segmentation, Graph theory, Min-cut/max-flow, Feature space.**

I. Introduction

IMAGE segmentation is a crucial problem in machine vision. Therefore it has been widely studied over the years and numerous distinctly different approaches to image segmentation have already been proposed.

Recent research on image segmentation has seen an increasing interest in graph based techniques which preform object extraction by partitioning graph based image representation into sub-graphs.

The most representative methods for graph based image segmentation are: (i) spectral graph partitioning using the eigenvectors of the graph Laplacian to partition the graph [1] and (ii) combinatorial graph cuts which perform segmentation by solving min-cut/max-flow problem [2,3]. Spectral graph partitioning methods are problems of NP-complexity and they are too slow for practical applications of machine vision. Therefore they will not be considered in this paper.

The main attention of this paper is focused on these image segmentation methods which use combinatorial graph cuts. Specifically, an extension of min-cut/max-flow method introduced in [2] is proposed. The main change of the proposed approach is to regard neighborhood in feature space rather than spatial neighborhood of adjacent pixels as in case the original method.

The following part of this paper is organized as follows. Firstly, in Section 2 graph representation of an image is explained. Next, in Section 3 the glance at min-cut/max-flow image segmentation is given. This is followed in Section 4 by the description of the proposed approach. Results of this approach are presented and compared with the source method in Section 5. Some of the computational issues are discusses in Section 6. Finally, Section 7 concludes the paper.

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II. Graph-based Image Representation

Digital image can be considered as a weighted graph with pixels represented by nodes $v_i \in V$ connected by edges $e_{ij}=\{v_i, v_j\} \in E$. Each edge has the nonnegative weight w_{ij} which describes similarity between the incident nodes. Regarding graph based image representation image segmentation is a partitioning of graph $G=(V, E)$ into two disjoint sets A and B where $A \cup B=V$ and $A \cap B=\emptyset$. The partitioning is performed according to some criterion and aims at removing edges that connect subgraphs A and B (see Fig. 1).

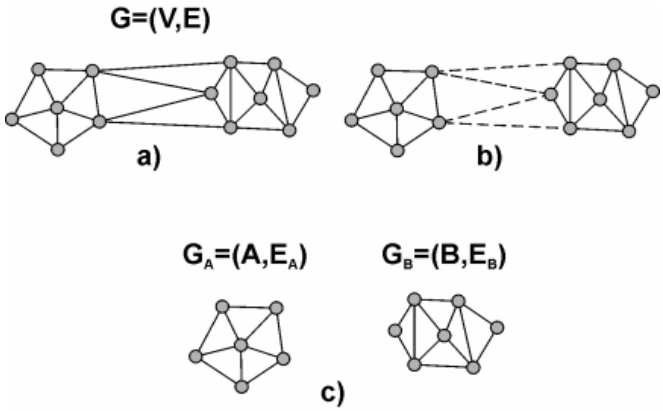

Fig. 1. Graph partitioning; (a) input graph G; (b) edges to be removed are denoted by dashed lines; (c) disjoint subgraphs G_A and G_B

III. Min-Cut/Max-Flow Image Segmentation

A. Min-Cut/Max-Flow Theorem

A cut (S, T) of a directed graph is a set of edges $C \in E$ such that the two terminals become separated on the induced graph $G'=(V, E/C)$. Minimal cut (min-cut) is a cut of minimum total capacity. According to min-cut/max-flow theorem the minimal cut is equal to maximum flow that can

be passed from the source S to sink T [4]. This concept is presented in Figure 2.

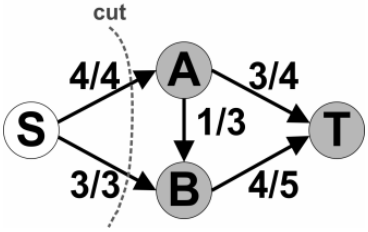

Fig. 2. An idea of min-cut/max-flow theorem. The maximum flow is equal to a total capacity of minimal cut C ={{S,A},{S,B}}

B. *Graph-Cut Image Segmentation*

The inspiration of the approach presented in this paper was min-cut/max flow segmentation proposed in [2]. In this method an image is represented by a weighted and undirected graph $G=(V,E)$. The set of nodes $V=P\cup\{S,T\}$ consists from subset P of nodes corresponding with pixels and two terminal nodes: the object terminal S (source) and the background terminal T (sink). The set E of edges consists of two types of undirected edges: *n-links* which connect neighboring pixels and *t-links* which connect pixels with the terminals. Every pixel has up to four *n-links* to the closest, neighboring pixels and two *t-links*: {p, S} and {p, T} connecting it to source and sink respectively. Exemplary graph obtained for 3×3 image is shown in Figure 3.

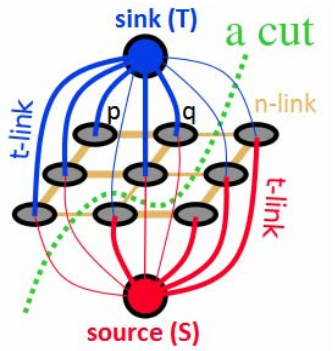

Fig. 3. Exemplary graph obtained for 3×3 image [2]

Weights $B_{\{pq\}}$ assigned to *n-links* represent boundary term and describe similarity between the neighboring nodes p and q. The higher the weight - the higher similarity between pixels. Weights $R_p(\cdot)$ assigned to *t-links* represent regional term and define the individual penalties R_p("obj") and R_p("bkg") for assigning pixel p to object and background respectively. The weights of edges suggested by Boykov and Jolly are given in Table I,
where:

$$K = 1 + \max_{p\in P} \sum_{q:\{p,q\}} B_{\{p,q\}} \qquad (1)$$

and λ is a scaling factor indicating the importance of regional term versus boundary term.

Having the graph defined above image segmentation is defined by the edges which get saturated when maximum flow is send from terminal S to terminal T. The maximum flow is determined using an efficient algorithm based on augmenting paths proposed in [3].

TABLE I
WEIGHTS FOR N-LINKS AND T-LINKS

Edge	Weight	For
$\{p, q\}$	$B_{\{pq\}}$	$\{p, q\} \in N$
$\{p, S\}$	$\lambda \cdot R_p$("bkg")	$p \in P, p \notin OB$
	K	$p \in O$
	0	$p \in B$
$\{p, T\}$	$\lambda \cdot R_p$("obj")	$p \in P, p \notin O \cup B$
	0	$p \in obj$
	K	$p \in bkg$

IV. THE PROPOSED APPROACH

The main idea of the approach proposed in this paper is to modify Boykov and Jolly's method by replacing spatial neighborhood of pixels with the neighborhood in a feature space. Specifically, in the graph representing input image *n-links* connect neighbors in the feature space i.e. the most similar pixels according to some similarity measure. These are not necessarily the adjacent pixels.

In the graph every pixel $p \in P$ can have up to $k+MN$ *n-links*: k connecting it to its k-nearest neighbors, and up to MN ones coming from pixels which found the pixel p to be its nearest neighbor (MN are image dimensions). If there are more than needed equally similar pixels, consecutive neighbors are chosen randomly.

The idea of graph construction using the proposed method is explained in Figure 4. Specifically, Figure 4a shows exemplary 3×3 image. Intensity of each pixel is given with bold font. Additionally, number (id) of the node corresponding with every pixel is given in brackets. Figure 4b presents adjacency matrix obtained for spatial adjacency graph as proposed by Boykov and Jolly, where each pixel is connected with up to 4 adjacent pixels. 1's denote that nodes of a given ids are connected by *n-links*; lack of connection between nodes is denoted by 0's. Graph adjacency matrix obtained for the proposed approach is shown in Figure 4b. The graph was built with regard that each pixel is connected to its 4 closest (with respect to intensity) neighbors.

It should be mentioned, that connecting pixels according to their similarities, makes *n-links* directed edges. It's because the neighborhood in a feature space is not always symmetric (as in case of the spatial neighborhood). This may be observed from graph adjacency matrices shown in Figure 4.

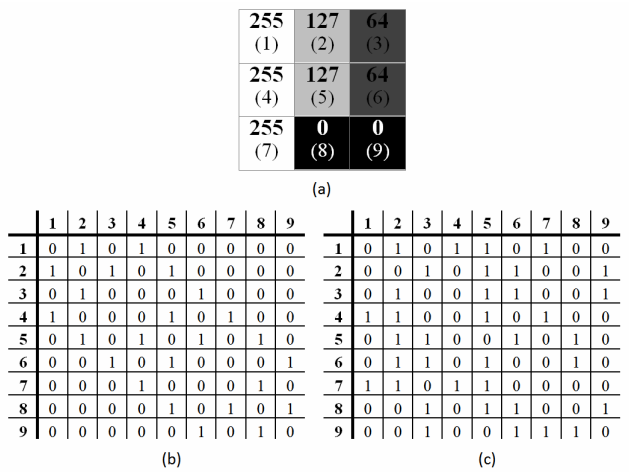

Fig.4. Idea of connecting pixels via *n-links*; (a) exemplary image 3×3; (b) graph adjacency matrix obtained for a spatial neighborhood; (c) graph adjacency matrix obtained for a neighborhood in a feature space for 4 nearest neighbors with respect to pixel intensities

It should be mentioned, that connecting pixels according to their similarities, makes *n-links* directed edges. It's because the neighborhood in a feature space is not always symmetric (as in case of the spatial neighborhood). This may be observed from graph adjacency matrices shown in Figure 4.

Weights $B_{\{pq\}}$ assigned to *n-links* in the proposed approach are determined with respect to Euclidean distance $d(p,q)$ in the feature space. Specifically, they are given by following equation:

$$B_{\{p,q\}} = \begin{cases} \infty & for\ e_{pq} \notin E \\ e^{-\frac{d(p,q)}{\sigma}} & for\ e_{pq} \in E \end{cases} \quad (2)$$

where

$$d(p,g) = \sqrt{\sum_i (p_i - q_i)^2} \quad (3)$$

Additionally, σ is some scaling factor and p_i is a i-th feature describing pixel p.

Weights assigned to *t-links* describe probabilities that each pixel belongs to background and foreground and are described by the following equations:

$$R_p("obj") = -\ln \Pr(I_p \,|\, "obj") \quad (4)$$

$$R_p("bkg") = -\ln \Pr(I_p \,|\, "bkg") \quad (5)$$

where I_p denotes intensity of pixel p and probability Pr is determined based on intensity distribution in regions of object and background indicated by the user.

V. Results

This section shows results of applying the proposed approach to exemplary 8-bit grey-scale images from Figure 5. Specifically, images of *frog* (Fig. 5a), *yarn* (Fig. 5b), *tree* (Fig. 5c), *brain* (Fig. 5d) and *plane* (Fig. 5e) are considered. Spatial resolution of regarded images do not exceed 256×256 pixels.

During the experiments every pixel was described by three features: its intensity, average intensity in 3×3 neighborhood and the corresponding variance of the intensity.

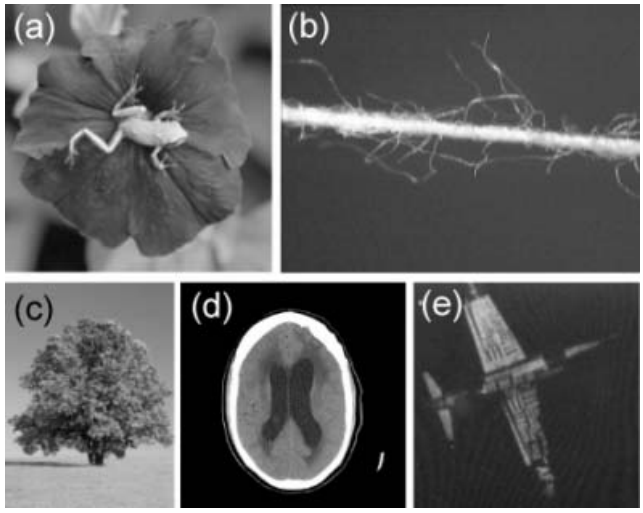

Fig.5. Exemplary images (a) *frog*; (b) *yarn*; (c) *tree*; (d) *brain*; (e) *plane*

Results of applying the proposed method to exemplary images are shown and compared with results of min-cut/max-flow segmentation in Figure 6. Specifically, the

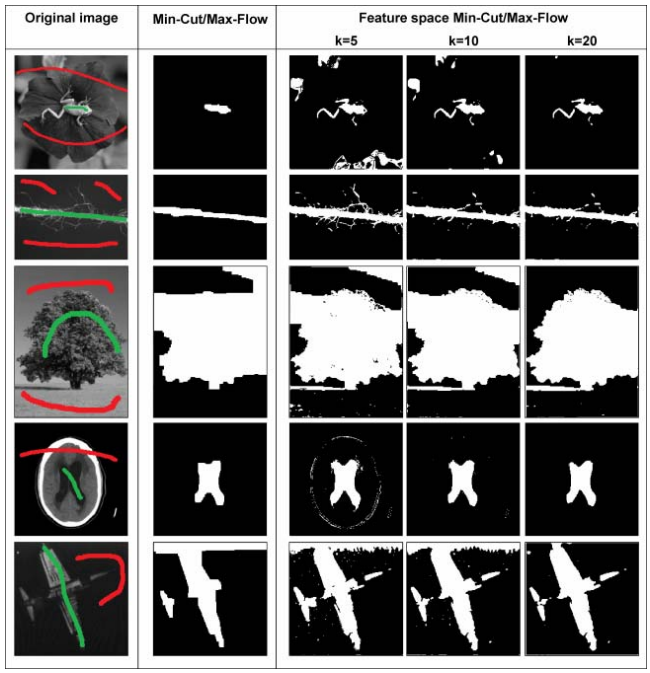

Fig.6. Results of image segmentation using the proposed method compared to results provided by Boykov and Jolly's algorithm

first column presents input image with conditions imposed by the user on background and foreground. Green lines indicate pixels which must be included into the object. Similarly, red lines indicate regions belonging to the background. In the second column results provided by Boykov and Jolly's algorithm are shown. The remaining

columns present segmentation results obtained using the proposed approach for an increasing number k={5,10,20} of nearest neighbors used to build the graph.

Firstly, it should be noticed, that the main parameter influencing performance of the proposed method is a number k of nearest neighbors used to build the graph. Changing value of k allows to adjust accuracy of image segmentation. Including more neighbors from the feature space into the graph increases the compactness of the result and allows to eliminate regions of slightly lower similarity from the resulting image.

It can also be observed, that (regardless of number of neighbors used to build the graph) performing graph cuts in the feature space as proposed in this paper increases quality of image segmentation. While the segmentation using the graph build with regard to spatial adjacency allows to obtain only the coarse shape of the objects, application of the proposed approach increases the level of details present in the output image. This can be observed for example in case of *yarn* image where the proposed method extracted both – the yarn core and the protruding fibers or in case of *frog* image, where the proposed method extracted not only the frog trunk, but legs as well.

VI. Computational Issues

The proposed algorithm requires nearest neighbor searching. This makes it more computationally complex and time consuming, than the source method proposed by Boykov and Jolly which just checks four adjacent pixels. Using the brute force solution for nearest neighbors searching drastically increases time of image segmentation. However, the proposed approach usually requires a small, fixed number of neighbors which can be found efficiently using the approximate nearest neighbor searching algorithm and the corresponding ANN library [5]. As a result, a running time of the proposed method is less than 30 seconds for an image sized 256×256 pixels (Intel Core i7 3,2GHz, 12 GB RAM).

VII. Conclusions

In this paper problem of graph-based min-cut/max flow image segmentation was considered. The new approach was proposed. It regards neighborhood in the feature space during graph construction rather than the spatial neighborhood of pixels as in case of grid graphs used by the previous approaches. This allow to capture non-local properties of images and obtain more accurate image segmentation for a wide spectrum of different images.

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Method for Automated Synthesis of Micromodels of Plate Based Elements of MEMS

Vasyl Teslyuk, Rostyslav Kryvyy

Abstract – **In the article the method for automated design of micromodels of MEMS' elements based on developed micromodels on the basis of thin plates theory, developed algorithms and production rules is developed.**

Keywords: **MEMS, automated synthesis, пластинчасті елементи МЕМС.**

I. Introduction

Nowadays interdisciplinary scientific fields are actively developed. One of such fields is the microelctromechanic systems [1-3]. The peculiarity of these devices is the micron sizes that greatly complicate the process of their projection, testing, making experiments, production etc. That is why the programming systems, technologies, methods and models become playing essential role, enabling to obtain modeling and projection results with high accuracy and to automate the design of different functional appointment models.

II. Design of synthesis algorithm of micromodels of plate construction of MEMS elements

Micromodels of plate constructions of MEMS elements are developed and presented in a number of scientific studies [1, 4, 5]. Mostly, they all are based on thin plate theory, where differential equations are used for their description. They are grouped in the Table I. The code is assigned to every differential equation, and their physical processes are described too. The analogical procedure is carried out to critical (Table II) and initial conditions (Table III).

The synthesis process of micromodels of MEMS acoustic elements is in sequent choice of appropriate elements from presented tables. The algorithm of differential equations choice of critical and initial conditions is illustrated at Fig. 1. The choice is implemented on the basis of production rules, the general structure of which is viewed below. These rules are located in appropriate library and used by analysis block of proposed algorithm.

TABLE I

№	Type of differential equation	Code
1	$\frac{\partial^4 w(x,y)}{\partial x^4}+\frac{\partial^4 w(x,y)}{\partial x^2\partial y^2}+\frac{\partial^4 w(x,y)}{\partial y^4}=\frac{P}{D}$	Riv_1
2	$\left(\frac{\partial^2}{\partial r^2}+\frac{1}{r}\frac{\partial}{\partial r}\right)\left(\frac{\partial^2 w(r)}{\partial r^2}+\frac{1}{r}\frac{\partial w(r)}{\partial r}\right)=\frac{P(r)}{D}$	Riv_2
3	$D\frac{\partial^4 w(x,y,t)}{\partial x^4}+2D\frac{\partial^4 w(x,y,t)}{\partial x^2\partial y^2}+D\frac{\partial^4 w(x,y,t)}{\partial y^4}-$ $-k\frac{\partial w(x,y,t)}{\partial t}-\rho h\frac{\partial w^2(x,y,t)}{\partial t^2}=P(t)$	Riv_3
4	$D\frac{\partial^4 w(x,y)}{\partial x^4}+2D\frac{\partial^4 w(x,y)}{\partial x^2\partial y^2}+D\frac{\partial^4 w(x,y)}{\partial y^4}-$ $-(1-\upsilon)\left(\frac{\partial^2 D}{\partial y^2}\frac{\partial^2 w(x,y)}{\partial x^2}-2\frac{\partial^2 D}{\partial x\partial y}\frac{\partial^2 w(x,y)}{\partial x\partial y}+\frac{\partial^2 D}{\partial x^2}\frac{\partial^2 w(x,y)}{\partial y^2}\right)=P$	Riv_4
. .	. . .	. . .
n	$D_x\frac{\partial^2 w(x,y)}{\partial x^4}+2(D_0+2D_{xy})\frac{\partial^2 w(x,y)}{\partial x^2\partial y^2}+D_y\frac{\partial^4 w(x,y)}{\partial y^2}=P$	Riv_n

TABLE II

№	Type of critical conditions	Code
1	$w\big\vert_{\tilde{A}\tilde{D}}=w_0=w$	Gran_1
2	$\left.\frac{\partial w}{\partial n}\right\vert_{\tilde{A}\tilde{D}}=0$	Gran _2
…	…	…
m	$\left.\frac{\partial w}{\partial y}\right\vert_{\text{гр}}=qM_y,\ M_y=-D\left(\frac{\partial^2 w}{\partial y^2}+\nu\frac{\partial^2 w}{\partial x^2}\right)$	Gran _m

TABLE III

№	Type of initial conditions	Code
1	$w(x, y, t=0)=$	Poch_1
2	$\frac{\partial w(x,y,t=0)}{\partial t}=0$	Poch _2
. . .	. . .	. . .
к	$\left.\frac{\partial w(R,t=0)}{\partial n}\right\vert_{zp}=0$	Poch _к

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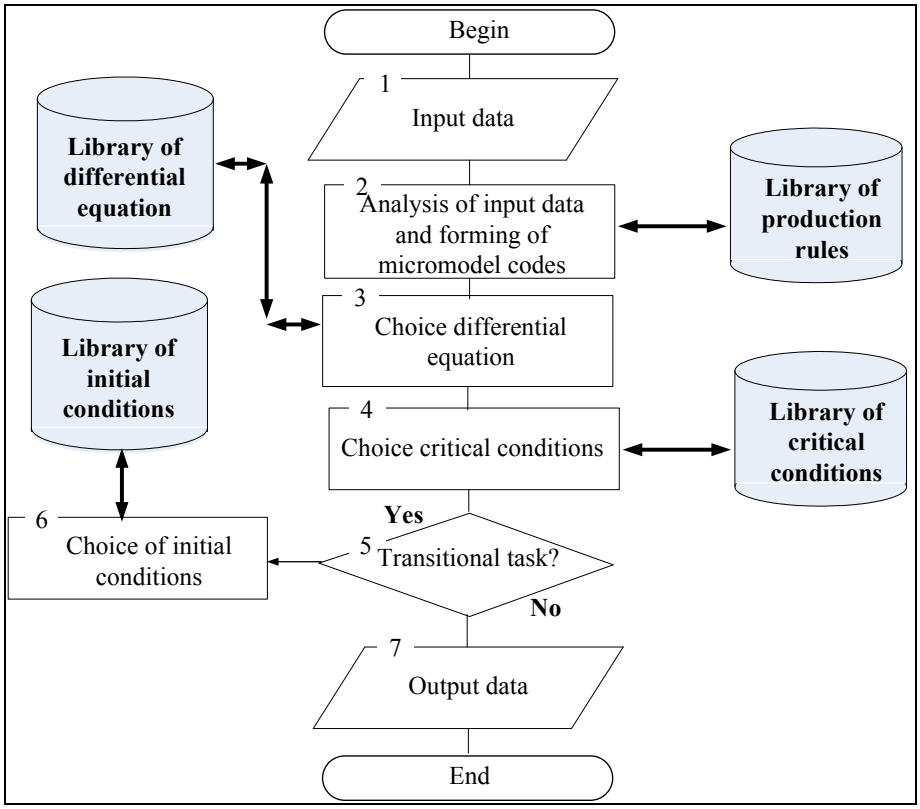

Fig. 1. Algorithm for automated synthesis of model plate MEMS elements

III. Design the algorithm of micromodels use of MEMS plate elements

The realization of previously mentioned models at your computer and their application for analysis and synthesis of MEMS plate elements requires the design of appropriate algorithms. At Fig. 2 the developed block-scheme of the algorithm of automated micromodel choice is presented for analysis and synthesis of microelectromechanic systems' elements.

During the first stage of algorithm usage some data should be inputted: basic construction, applied materials etc.

The basic construction and applied materials are choosing accordingly to Data base. On the basis of input task analysis and selected constructions and materials the micromodel code is formed. The further calculation of output parameters is carried out based on the micromodel.

However, within the use of crystalline silicon plates as material, which is anisotropic material, we ought to apply the appropriate micromodel (differential equation (Riv_n) with conditions (Gran_1); if it is necessary to increase the results acurancy we use the critical conditions of type (Gran_m)). In case of changeable of plate thickness of applied elements we use the differential equation (Riv_4) with critical conditions (Gran_1) or (Gran_m). If necessary to take into account the dynamics of output parameters change we use transitional micromodels. Dependently on plate construction it is used model based on differential equation (Riv_3) and appropriate critical and initial conditions.

In necessary to use the stationary model dependently on plate construction: for circular we use differential equation (Riv_2) with critical conditions (Gran_1 and Gran_2), and for orthogonal – the critical conditions (Gran_1), (Gran_2).

After analysis the results are presented at the monitor or in the suitable file for user

The offered algorithm makes possible in automated regime to analyze plate construction of MEMS elements, which use the thin plate as working elastic element

IV. Design of production rules

During the choice of differential equations of micromodels we use such type of production rules [6]:

PravRiv1: when $U_1 = A_1$, then $Code\_Riv = Riv\_1$;

PravRiv2: when $U_2 = A_2$, then $Code\_Riv = Riv\_2$;

…

PravRivn: when $U_n = A_n$, then $Code\_Riv = Riv\_n$,

where A_n - linguistic terms ; Riv_n - code of differential equation.

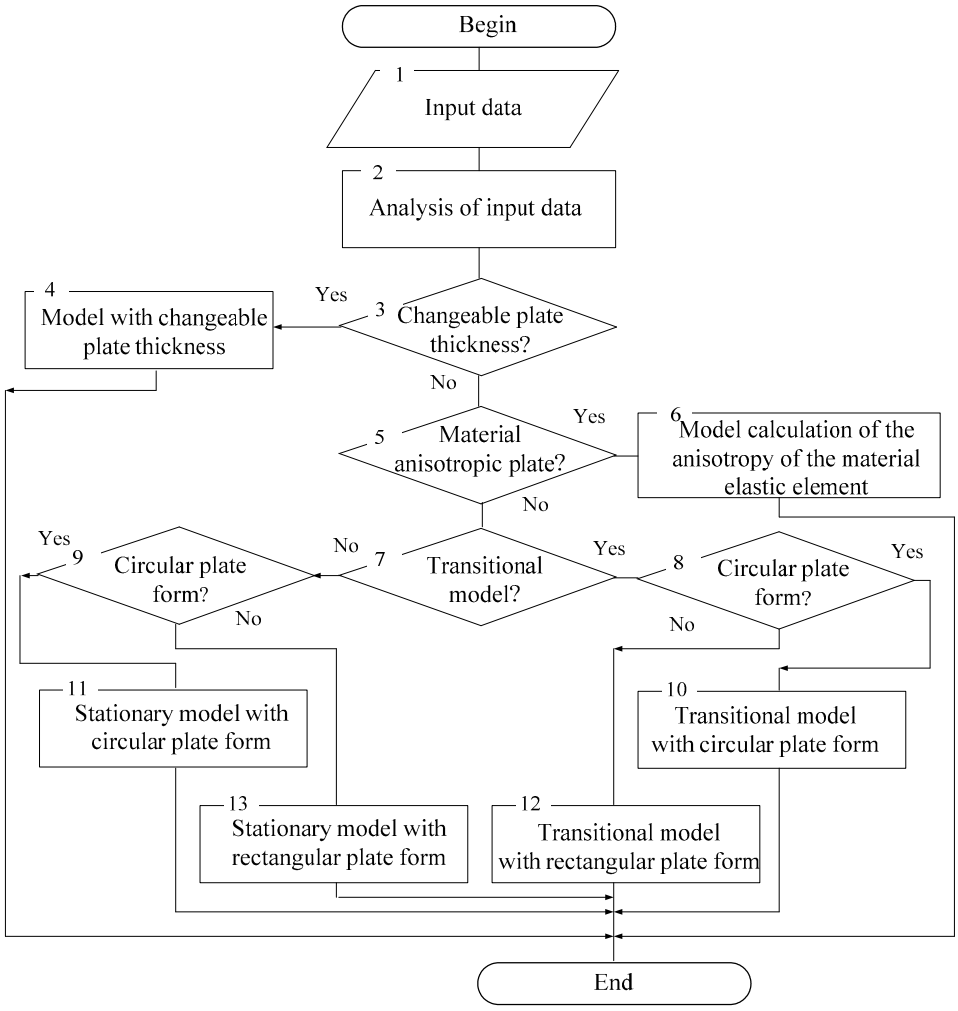

Fig.2. Algorithm for automatic selection of models

In case of choosing the critical conditions of micromodels it is used the analogical production rules:

PravGran1: when $Z_1 = B_1$, then $Code\_Gran = Gran\_1$;

PravGran2: when $Z_2 = B_2$, then $Code\_Gran = Gran\_2$;

…

PravGranm: when $Z_m = B_m$, then $Code\_Gran = Gran\_m$, where B_m – linguistic terms; $Gran\_m$ – code of critical condition.

For example, for calculation of material anisotropy it is used such production rule: if $U_1 = A_n$ then $Code\_Riv = Riv\_n$, $Code\_Gran = Gran\_1$..

Besides, we can change the critical condition if it is needed to raise the output results' accuracy.

For transitional micromodels it is necessary to add initial condition, selected with help of such production rules:

PravPoch1: when $X_1 = C_1$, then $Code\_Poch = Poch\_1$;

PravPoch2: when $X_2 = C_2$, then $Code\_Poch = Poch\_2$;

…

PravPochk: when $X_k = C_k$, then $Code\_Poch = Poch\_k$, де C_k – linguistic terms; $Poch\_k$ – coed of initial condition.

In some cases, it is used more comprehensive construction of production rules, which can used for micromodel synthesis within several critical and initial conditions:

PravGran_m+1: if $Z_{m+1} = B_{m+1}$, then $Code\_Gran = Gran\_1$, $Code1\_Gran = Gran\_4$.

For description of MEMS elements construction and micrimodels we built information model of XML format [7, 8]. The example of file with micromodel description of MEMS acoustic element is viewed at Fig. 3-4.

In illustrated example (Fig. 3) 1 and 2 strings describe the type of project. The 3-8 strings define the model, methods and main parameters of modeling. The 9-23 strings describe the microelements' sizes and the step mesh partitioning at finite differences.

```
01: <task name="Прогин  Мембрани">
02:       <description>Визначення переміщень та напружень у
    мембрані</description>
03:       <model> Акустичний елемент </model>
04:       <method> скіннчених  різниць</method>
05:       <simulation id="ПрогинМембрани" type="state analysis">
06:                 <parameter name="BottomBoundary"> Normal
    скінченіРізниці </parameter>
07:                 <property name="MeshAccuracy">0.01</property>
08:                 <property name="ConvergenceAccuracy">0.01</property>
09:                 <space type="regular grid">
10:                       <x>
11:                             <begin>0</begin>
12:                             <end>2E-3</end>
13:                             <step>1E-5</step>
14:                       </x>
15:                       <y>
16:                             <begin>0</begin>
17:                             <end>2E-3</end>
18:                             <step>1E-5</step>
19:                       </y>
20:                       <z>
21:                             <begin>0</begin>
22:                             <end>5E-5</end>

23:                       </z>
24:                 </space>
25:       </simulation>
26: </task>
```

Fig. 3..An example of the formalization of structure MEMS acoustic element using XML-format

The information model at Fig. 4 describes the micromodel of MEMS acoustic elements. The 1-st, 2-d strings have the model name and its description. The 3-6 strings are viewing the microsystem type. The construction of modeling device is described by 7-11strings., where the construction type, material and its sizes are presented. The 12-24 strings display the used mathematical model for modeling (coeds of initial and critical conditions, coed of differential equation).

```
01:   <Model name = Acus1>
02:         <description>  Model Acustyka MEMS1 </description>
03:         <typeMEMS>
04:               type = (electrostatic);
05:               clearance=5E-6;
06:         </typeMEMS>
07:         <konstruct >
08:               kon_typ=2;
09:               material=SiO2;
10:               rozmir (S,D,H) := 'C:\Documents\kons_v1.xml';
11:         </konstruct >
12:         <poch>
13:               t: { };
14:         </poch>
15:         <gran>
16:               x: {Gran_1, Gran_2};
17:               y: {Gran_1, Gran_2};
18:         </gran>
19:         <matem>
20:               mod1=Riv_1;
21:               g_x: mod2=Riv_5;
22:               g_y: mod3=Riv_6;
23:               t_xy: mod4=Riv_7;
24:         </matem>
25:   </Model>
```

Fig. 4. Example descriptions model MEMS acoustic element using XML - forma

V. Conclusion

Method for automated synthesis of micromodels of basic elements of MEMS plate design based on thin plates theory and designed production rules based. Structure of output files (designs and micromodels) with the description of synthesized model with XML representation has been designed.

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Mathematical and Numerical Modeling of Natural Convection in an Enclosure Region with Heat-conducting Walls by the R-functions and Galerkin Method

Artyukh A.

***Abstract*—This paper is dedicated to the investigation of the natural convection in an enclosed region. The mathematical model has been formulated using the dimensionless variables for the stream function and temperature. The numerical results have been obtained by means of the R-functions and Galerkin methods.**

***Index Terms*—natural convection, stream function, temperature, R-functions method, Galerkin method.**

I. Introduction

The problem of the natural convection in an enclosed region has vital importance in many technical applications such as microelectronics, radio electronics, energetics etc. Obviously, such problem has a lot of important implications which makes the corresponding investigation actual.

Such problems are mainly resolved using the finite difference and finite element methods. They are easy to program, but they are not universal since a new grid generation is required every time a transition to a new area is made. The R-functions method developed by the academician of the Ukrainian Academy of Sciences V. L. Rvachev allows considering the geometry of the problem accurately [5].

The objective of this work is the mathematical simulation of the natural convection in an enclosed region by means of the R-functions method and Galerkin method.

II. Problem Statement

The mathematical model of the natural convection in an enclosed region with heat-conducting walls in an arbitrary closed region is shown in Fig.1.

Let's consider the $\Omega = \Omega_s \bigcup \Omega_f$ area, where Ω_f is the gas cavity, Ω_s – solid walls, $\partial\Omega_{sf}$ – impermeable and fixed bound between Ω_f and Ω_s. It is assumed that the fluid is Newtonian, incompressible, and viscous.

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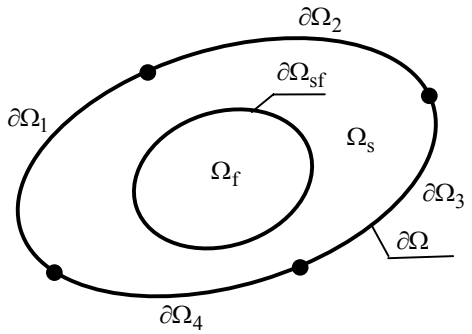

Fig. 1. Problem Solution Region

The mathematical model using the dimensionless variables takes the following form [3]:

in the cavity:

$$\frac{\partial\Delta\psi}{\partial\tau}+\frac{\partial\psi}{\partial y}\frac{\partial\Delta\psi}{\partial x}-\frac{\partial\psi}{\partial x}\frac{\partial\Delta\psi}{\partial y}=\sqrt{\frac{\mathbf{Pr}}{\mathbf{Ra}}}\Delta^2\psi+\frac{\partial\theta}{\partial x}, \quad (1)$$

$$\frac{\partial\theta}{\partial\tau}+\frac{\partial\psi}{\partial y}\frac{\partial\theta}{\partial x}-\frac{\partial\psi}{\partial x}\frac{\partial\theta}{\partial y}=\frac{1}{\sqrt{\mathbf{Ra}\cdot\mathbf{Pr}}}\Delta\theta, \quad (2)$$

in the solid walls:

$$\frac{\partial\theta}{\partial\tau}=\frac{a_{sf}}{\sqrt{\mathbf{Ra}\cdot\mathbf{Pr}}}\Delta\theta, \quad (3)$$

Where x, y are the dimensionless coordinates,

τ – dimensionless time,

Δ – Laplace operator,

ψ – dimensionless stream function,

θ – dimensionless temperature,

$\mathbf{Ra}=\frac{g\beta TL^3}{\nu a_f}$ – Rayleigh number,

$\mathbf{Pr}=\frac{\nu}{a_f}$ – Prandtl number,

g – acceleration of gravity,

β – coefficient of volumetric thermal expansion,

ν – kinematic coefficient of viscosity,

a_f – temperature diffusivity coefficient of the gas,

$a_{sf} = \frac{a_{solid}}{a_{fluid}}$ – relative temperature diffusivity coefficient,

$\lambda_{sf} = \frac{\lambda_{solid}}{\lambda_{fluid}}$ – relative heat conduction coefficient,

L – length of the gas cavity.

Equation (1) is considered for Ω_f, and equations (2) – (3) are considered for Ω_f and Ω_s respectively.

Initial conditions for the problem (1) – (3) are set as follows:

$$\psi\big|_{\tau=0} = \psi_0(x, y), \quad (4)$$

$$\theta\big|_{\tau=0} = \theta_0(x, y). \quad (5)$$

The boundary conditions have the following form:

at external borders:

$$\theta\big|_{\partial\Omega_1} = \theta_1, \quad \theta\big|_{\partial\Omega_3} = \theta_2, \quad (6)$$

$$\left.\frac{\partial\theta}{\partial\vec{n}}\right|_{\partial\Omega_2} = 0, \quad \left.\frac{\partial\theta}{\partial\vec{n}}\right|_{\partial\Omega_4} = 0, \quad (7)$$

at internal borders:

$$\psi\big|_{\partial\Omega_{sf}} = 0, \quad \left.\frac{\partial\psi}{\partial\vec{n}}\right|_{\partial\Omega_{sf}} = 0, \quad (8)$$

$$\theta_s = \theta_f, \quad \frac{\partial\theta_f}{\partial\vec{n}} = \lambda_{sf}\frac{\partial\theta_s}{\partial\vec{n}} \text{ on } \partial\Omega_{sf}, \quad (9)$$

where $\partial\Omega = \partial\Omega_1 \cup \partial\Omega_2 \cup \partial\Omega_3 \cup \partial\Omega_4$, θ_s – temperature in the solid wall, θ_f – temperature in the gas cavity, $\vec{n}$ is a normal vector to the boundary.

III. The R-functions Method

Consider the inverse problem of analytical geometry. Let's consider a geometric object Ω in space R^2 with a piecewise smooth bound $\partial\Omega$. It is required to construct a function $\omega(x, y)$ that would be positive inside Ω, negative outside of Ω and equal to zero at $\partial\Omega$. The equation The equation $\omega(x, y) = 0$ determines an implicit form of the locus for the points that belong to the boundary $\partial\Omega$ of the region Ω.

Definition 1. The function with the sign entirely determined by the signs of its arguments is called the R-function corresponding to the partition of the numerical axis within the $(-\infty, 0)$ and $[0, +\infty)$ intervals, i.e. the function $z = f(x, y)$ is called the R-function if the Boolean function F exists and $S[z(x, y)] = F[S(x), S(y)]$, where $S(x)$ is a double-valued predicate $S(x) = \begin{cases} 0, & x < 0, \\ 1, & x \geq 0. \end{cases}$

The $\Re_\alpha$ is the most widespread R-function system:

$$x \wedge_\alpha y \equiv \frac{1}{1+\alpha}(x + y - \sqrt{x^2 + y^2 - 2\alpha xy}),$$

$$x \vee_\alpha y \equiv \frac{1}{1+\alpha}(x + y + \sqrt{x^2 + y^2 - 2\alpha xy}),$$

$$\overline{x} \equiv -x,$$

where

$-1 < \alpha(x, y) \leq 1$, $\alpha(x, y) \equiv \alpha(y, x) \equiv \alpha(-x, y) \equiv \alpha(x, -y)$.

Let's consider the Ω region that can be created based on simpler regions $\Omega_1 = \{\omega_1(x, y) \geq 0\}, \ldots, \Omega_m = \{\omega_m(x, y) \geq 0\}$, by means of the of set-theoretic operations such as union, intersection and complement. Therefore, let's assume that the predicate

$$\Omega = F(\Omega_1, \Omega_2, \ldots, \Omega_m) \quad (10)$$

corresponding to the region Ω is equal to 1 if $(x, y) \in \overline{\Omega}$ and is equal to 0 if $(x, y) \notin \overline{\Omega}$.

The transition from the predicate-based form of the region defining (10) to an ordinary analytical geometry equation is made using the formal substitution of Ω with $\omega(x, y)$, Ω_i with $\omega_i(x, y)$ $(i = 1, 2, \ldots, m)$, and the $\{\cap, \cup, \neg\}$ are substituted with the R-operations symbols $\{\wedge_\alpha, \vee_\alpha, -\}$ respectively. As a result, an analytic expression for $\omega(x, y)$ is derived. This expression defines the required equation $\omega(x, y) = 0$ of the bound $\partial\Omega$ for the elementary functions. Note that $\omega(x, y) > 0$ for the interior points and $\omega(x, y) < 0$ for the exterior points of Ω.

Definition 2. The equation $\omega(x, y) = 0$ for the bound $\partial\Omega$ of $\Omega \subset R^2$ is normalized to the order n if the function $\omega(x, y)$ satisfies these conditions: $\omega\big|_{\partial\Omega} = 0$, $\left.\frac{\partial\omega}{\partial\vec{n}}\right|_{\partial\Omega} = -1$, $\left.\frac{\partial^k\omega}{\partial\vec{n}^k}\right|_{\partial\Omega} = 0$ $(k = 2, 3, \ldots, n)$, where $\vec{n}$ is an outer normal vector to $\partial\Omega$, that is defined for all regular points of Ω.

The equation $\omega(x, y) = 0$ normalized to the first order can be obtained from the equation $\omega(x, y) = 0$ as described below.

Theorem 1. If $\omega(x, y) \in C^m(R^2)$ satisfies the conditions $\omega\big|_{\partial\Omega} = 0$ and $\left.\frac{\partial\omega}{\partial\vec{n}}\right|_{\partial\Omega} > 0$, then the function

$$\omega_1 \equiv \frac{\omega}{\sqrt{\omega^2 + |\nabla\omega|^2}} \in C^{m-1}(R^2), \quad |\nabla\omega| \equiv \sqrt{\left(\frac{\partial\omega}{\partial x}\right)^2 + \left(\frac{\partial\omega}{\partial y}\right)^2},$$

satisfies the conditions $\omega_1\big|_{\partial\Omega} = 0$ and $\left.\frac{\partial\omega_1}{\partial\vec{n}}\right|_{\partial\Omega} = -1$ for all regular points of the bound $\partial\Omega$.

We can use this simplified formula: $\omega \equiv \frac{\omega_1}{|\nabla\omega_1|}$ for the equation normalized to the first order if $|\nabla\omega_1| \neq 0$ in $\overline{\Omega} = \Omega \cup \partial\Omega$.

Let's consider the R-function application scheme for the boundary problems solving. The problem of the physical field calculation can be reduced to finding the solution u of the equation $Au = f$ within the region Ω under the following conditions on the bound $\partial\Omega$ of Ω: $L_i u = \varphi_i$, $i = 1, ..., m$, where A and L_i are known differential operators; f and φ_i – functions defined inside Ω and in the areas of its boundary $\partial\Omega$. The areas $\partial\Omega_i$ are not necessarily all different, and may coincide with the whole bound $\partial\Omega$. The functions u, f, φ_i and operators A and L_i mentioned in the boundary problem statement are called analytic components of the boundary problem, the area Ω, its boundary $\partial\Omega$, border areas $\partial\Omega_i$ are called geometric components.

The existence of two different types of information (analytical and geometrical) is a major obstacle for the solution finding. Not only the look of the formulas included into the problem statement should be considered, but the geometrical information should be transferred to the analytical look to so that it can be involved into the solution algorithm. The R-functions method allows this procedure implementation.

The sheaves of functions can be built by means of the normalized equations. The normal derivatives of such functions or an arbitrary linear combination of the normal derivative and the function itself take the given values on the region bounds.

In order to achieve this, let's consider the following operator

$$D_1 \equiv \frac{\partial\omega}{\partial x}\frac{\partial}{\partial x} + \frac{\partial\omega}{\partial y}\frac{\partial}{\partial y},$$

where $\omega(x, y)$ is a normalized equation of the region bound. Moreover, for any sufficiently smooth function f on the bound $\partial\Omega$ this statement will be valid:

$$D_1 f\big|_{\partial\Omega} = -\frac{\partial f}{\partial \vec{n}}\bigg|_{\partial\Omega},$$

where $\vec{n}$ is an outer normal vector to $\partial\Omega$.

Let

$$D_1^{(i)} \equiv \frac{\partial\omega_i}{\partial x}\frac{\partial}{\partial x} + \frac{\partial\omega_i}{\partial y}\frac{\partial}{\partial y}$$

denote the analog of D_1 corresponding to the areas $\partial\Omega_i$ of the bound $\partial\Omega$, where $\omega_i(x, y)$ are normalized equations of for the areas $\partial\Omega_i$.

One can prove that

$$D_1\omega = 1 + O(\omega),$$

$$D_1(\omega\Phi) = = (D_1\omega)\Phi + \omega D_1\Phi = \Phi + O(\omega),$$

where $\omega(x, y)$ is the normalized equation of the region bound.

Definition 3. The expression

$$u = B(\Phi,\ \omega,\ \{\omega_i\}_{i=1}^{m},\ \{\varphi_j\}_{j=1}^{m})$$

is called the general boundary problem solution structure if that expression exactly satisfies all boundary conditions of the problem for any undetermined component Φ chosen. B is the operator dependent on the geometry of the region and parts of its border, as well as on the operators of the boundary conditions, but is not dependent on the type of operator A and function f.

Let's consider the expression $u = B_i(\Phi,\ \omega,\ \omega_i,\ \varphi_j)$ as a partial solution structure that exactly satisfies the boundary condition only on $\partial\Omega_i$ for any undetermined component.

Thus, the solution structure provides extension of the boundary conditions into the region.

The task of the equation creation for the complex geometric object is a specific case of a more general problem where the unknown function φ takes the given values on different parts of the bound $\partial\Omega_i$, i.e.

$$\varphi = \varphi_i \text{ on } \partial\Omega_i,\ i = 1,\ ...,\ m. \qquad (11)$$

For simplicity, let's assume that φ_i are elementary functions defined everywhere in the region $\Omega \cup \partial\Omega$. After the methodology described above is applied, the functions ω_i^0 equal to zero everywhere, except for the area $\partial\Omega_i$ are constructed. Thus, the function

$$\varphi = \left(\sum_{i=1}^{m} \varphi_i \omega_i^0\right)\left(\sum_{j=1}^{m} \omega_j^0\right)^{-1} \qquad (12)$$

satisfies (11) and is defined everywhere in the region, with the exception of the points that are common to the different sections. Instead of (12) we can also apply the formula

$$\varphi = \left(\sum_{i=1}^{m} \varphi_i \omega_i^{-1}\right)\left(\sum_{j=1}^{m} \omega_j^{-1}\right)^{-1}, \qquad (13)$$

where $\omega_i = 0$ are equations of $\partial\Omega_i$ of the bound $\partial\Omega$, and $\omega_i > 0$ outside $\partial\Omega_i$. The function $\omega_i \to 0$ when approaching the area $\partial\Omega_i$ and the limit values of the function φ match the values of the corresponding function φ_i.

Let's denote the bonding operator for the boundary values defined by any of the above formulas (12) and (13) as EC $(EC\varphi_i = \varphi)$.

Practically all of the approximate methods for the boundary problems solving for the partial differential equations are based on the infinite-dimensional problem to a finite-dimensional one reducing. The method of R-

functions provides the corresponding result achieving by means of the undetermined component of the solution structure representation as the sum:

$$\Phi(x,y) \approx \Phi_n(x,y) = \sum_{k=1}^{n} c_k \varphi_k(x,y),$$

where $\varphi_k(x,y)$ are known elements of the complete functional sequence, and c_k $(k = 1,2,...,n)$ are unknown expansion coefficients.

The undefined functions included into the structural formulas should be chosen so that the basic differential equation of the problem is satisfied with the best results. The methods of the undefined function approximations search can be very different. For example, one can use the variational (Ritz, least squares, etc.), projection (Galerkin, collocation, etc.), grid and other methods.

IV. Solution Method

The R-functions and Galerkin methods are used for the initial-boundary problem (1) – (9) solving.

Let's consider the boundaries $\partial\Omega$ and $\partial\Omega_{sf}$ that are are piecewise smooth and that can be described by means of the elementary functions $\omega(x,y)$ and $\omega_{sf}(x,y)$. According to the R-functions method, $\omega(x,y)$ and $\omega_{sf}(x,y)$ satisfy the below conditions:

1) $\omega(x,y) > 0$ in Ω;

2) $\omega(x,y) = 0$ on $\partial\Omega$;

3) $\dfrac{\partial\omega}{\partial\vec{n}} = -1$ on $\partial\Omega$, $\vec{n}$ is an outer normal vector to $\partial\Omega$,

and

1) $\omega_{sf}(x,y) > 0$ in Ω_f;

2) $\omega_{sf}(x,y) = 0$ on $\partial\Omega_{sf}$;

3) $\dfrac{\partial\omega_{sf}(x,y)}{\partial\vec{n}} = -1$ on $\partial\Omega_{sf}$, $\vec{n}$ is a normal vector pointing into Ω_f.

The investigation in [5] shows that the boundary conditions (7) – (8) are satisfied by the sheaf of functions

$$\psi = \omega_{sf}^2 \Phi,$$

where $\Phi = \Phi(x,y,\tau)$ is an undefined component.

The solution structure of (2) – (3), i.e. the sheaf of functions which satisfies the boundary conditions (5), (6), (9), was built by means of the region-structure Rvachev-Slesarenko method [6]. Hence

$$\theta = \begin{cases} B(\Upsilon) \text{ in } \Omega_s, \\ B(\Upsilon) - (1-\lambda_{sf})\omega_{sf} D_1 B(\Upsilon) \text{ in } \Omega_f, \end{cases} \quad (14)$$

where $\Upsilon = \Upsilon(x,y,t)$ is an undefined component, $B(\Upsilon)$ satisfies the boundary conditions on external borders.

The undefined components Φ and Υ were found by means of the Galerkin method. Therefore, we will obtain an approximate solution of the problem (1) – (9).

V. Numerical Results

Let's consider the mathematical model of natural convection (1) – (3) in a closed region (fig. 2) [3]. It is assumed that the fluid is Newtonian, incompressible and viscous.

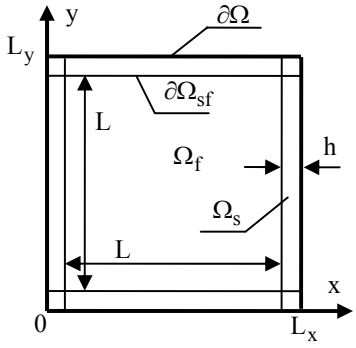

Fig. 2. Problem Solution Region

The initial conditions for the problem (1) – (3) have the below form:

$$\psi\big|_{\tau=0} = \theta\big|_{\tau=0} = 0. \quad (15)$$

The boundary conditions are set as follows:

on external borders:

$$\theta\big|_{x=0} = \theta_1, \quad \theta\big|_{x=L_x} = \theta_2, \text{ where } 0 \le y \le L_y, \quad (16)$$

$$\left.\frac{\partial\theta}{\partial\vec{n}}\right|_{y=0} = 0, \quad \left.\frac{\partial\theta}{\partial\vec{n}}\right|_{L_y} = 0, \text{ where } 0 \le x \le L_x, \quad (17)$$

on internal borders:

$$\psi\big|_{x=h} = \psi\big|_{x=L_x-h} = \psi\big|_{y=h} = \psi\big|_{y=L_y-h} = 0, \quad (18)$$

$$\left.\frac{\partial\psi}{\partial\vec{n}}\right|_{x=h} = \left.\frac{\partial\psi}{\partial\vec{n}}\right|_{x=L_x-h} = \left.\frac{\partial\psi}{\partial\vec{n}}\right|_{y=h} = \left.\frac{\partial\psi}{\partial\vec{n}}\right|_{y=L_y-h} = 0, \quad (19)$$

$$\theta_s = \theta_f, \quad \frac{\partial\theta_f}{\partial\vec{n}} = \lambda_{sf}\frac{\partial\theta_s}{\partial\vec{n}}. \quad (20)$$

where θ_s is the temperature in the solid wall, θ_f – temperature in the gas cavity, $\vec{n}$ – normal vector to the boundary, L_x and L_y are normalized by the length of the gas cavity L.

The functions $\omega(x,y)$ and $\omega_{sf}(x,y)$ have the following form:

$$\omega(x,y) = \frac{1}{L_x}x(L_x - x) \wedge_0 \frac{1}{L_y}y(L_y - y),$$

$$\omega_{sf}(x,y) =$$

$$= \frac{1}{L_x - 2h}(x-h)(L_x - x) \wedge_0 \frac{1}{L_y - 2h}(y-h)(L_y - y).$$

After (14) is applied, $B(\Upsilon)$ satisfies the boundary

conditions on external borders (16) – (17), i.e.

$$B(\Upsilon)\Big|_{\frac{x}{L_x}(L_x-x)=0} = \frac{\theta_1(L_x-x)+\theta_2 x}{L_x},$$

$$\frac{\partial B(\Upsilon)}{\partial \vec{n}}\Big|_{\frac{y}{L_y}(L_y-y)=0} = 0.$$

The basic functions used are power polynomials, trigonometric polynomials and Legendre polynomials. The Gauss formula with 16 knots was used for evaluation of integrals in the Galerkin method.

The stream lines, temperature field and vorticity field for $L_X = L_Y = L = 1$, $h = 0.05$, $\mathbf{Ra} = 10^3$, $\mathbf{Pr} = 0.7$, $\lambda_{sf} = 10$, $\theta_1 = 0.5$, $\theta_2 = -0.5$, $a_{sf} = 1$, $T = 5$ are given in figures 1, 2; 3, 4, and 5, 6 for different time respectively.

The results of numerical experiment well correspond to those obtained by the other authors [3].

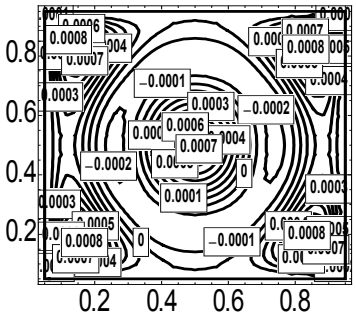

Fig. 3. Stream Lines $t = 0.02$

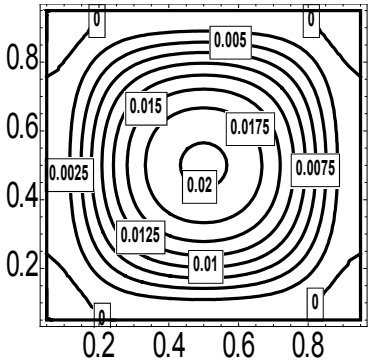

Fig. 4. Stream Lines $t = 3$

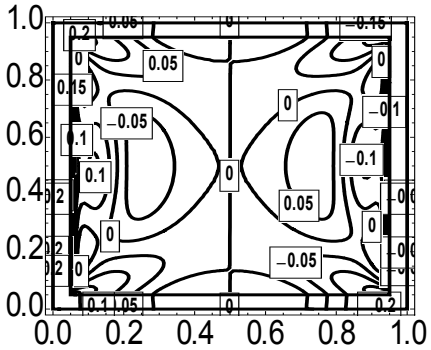

Fig. 5. Temperature Field $t = 0.02$

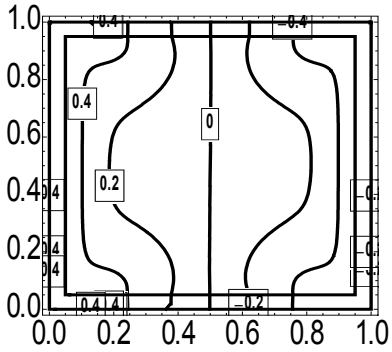

Fig. 6. Temperature Field $t = 3$

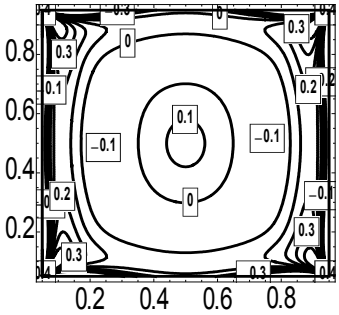

Fig. 7. Vorticity Field $t = 0.02$

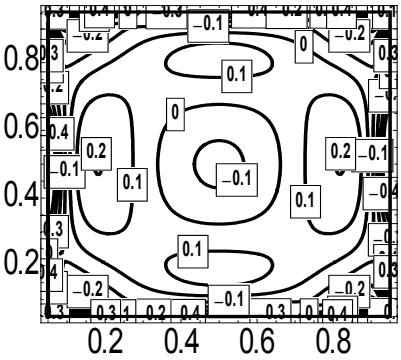

Fig. 8. Vorticity Field $t = 3$

VI. Conclusion

The natural convection in an enclosed region with the presence of local heat is investigated. The solution structures of unknown function were built by means of the R-functions method, and the Galerkin method was used for the approximate undefined components. Thus, the stream function and the temperature were represented in analytical way.

The algorithm for solving the problem of mathematical modeling and numerical analysis of non-stationary natural convection in an enclosed region based on the R-functions method and the Galerkin method is used. The advantage of the suggested algorithm is that it does not have to be modified for different geometries of the regions being reviewed which illustrates the scientific innovation of the results obtained. As a result, the approximate solution for

such streams investigation problems is obtained in the non-classic geometry field.

The methods developed for analysis of natural convection in an enclosed region are easy to use for the program algorithms and are more versatile than those used at the present time, as one only needs to change the boundary equation in order to make the transition from one region to another. The obtained results allow us to carry out computational experiments in mathematical modeling of various physical, mechanical, and biological streams.

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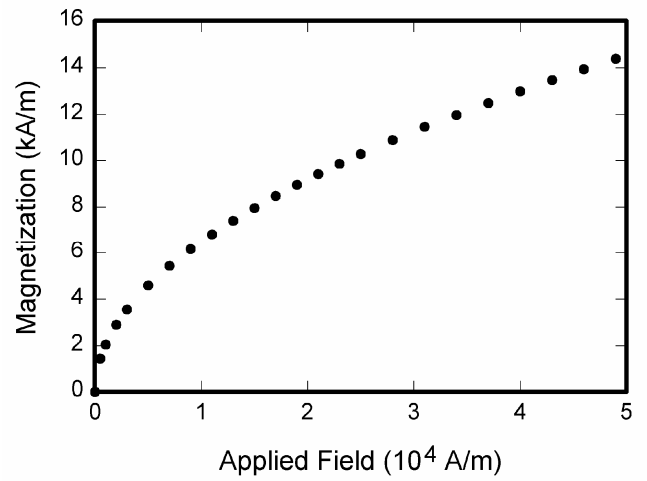

Fig. 1. Magnetization as a function of applied field. Note that "Fig." is abbreviated. There is a period after the figure number, followed by two spaces. It is good practice to explain the significance of the figure in the caption.

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TABLE I
UNITS FOR MAGNETIC PROPERTIES

Symbol	Quantity	Conversion from Gaussian and CGS EMU to SI [a]
Φ	magnetic flux	1 Mx $\rightarrow 10^{-8}$ Wb = 10^{-8} V·s
B	magnetic flux density, magnetic induction	1 G $\rightarrow 10^{-4}$ T = 10^{-4} Wb/m^2
H	magnetic field strength	1 Oe $\rightarrow 10^3/(4\pi)$ A/m
m	magnetic moment	1 erg/G = 1 emu $\rightarrow 10^{-3}$ A·m^2 = 10^{-3} J/T
M	magnetization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 10^3$ A/m
$4\pi M$	magnetization	1 G $\rightarrow 10^3/(4\pi)$ A/m
σ	specific magnetization	1 erg/(G·g) = 1 emu/g $\rightarrow$ 1 A·m^2/kg
j	magnetic dipole moment	1 erg/G = 1 emu $\rightarrow 4\pi \times 10^{-10}$ Wb·m
J	magnetic polarization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 4\pi \times 10^{-4}$ T
χ, κ	susceptibility	1 $\rightarrow 4\pi$
χ_ρ	mass susceptibility	1 cm^3/g $\rightarrow 4\pi \times 10^{-3}$ m^3/kg
μ	permeability	1 $\rightarrow 4\pi \times 10^{-7}$ H/m = $4\pi \times 10^{-7}$ Wb/(A·m)
μ_r	relative permeability	$\mu \rightarrow \mu_r$
w, W	energy density	1 erg/cm^3 $\rightarrow 10^{-1}$ J/m^3
N, D	demagnetizing factor	1 $\rightarrow 1/(4\pi)$

Vertical lines are optional in tables. Statements that serve as captions for the entire table do not need footnote letters.

[a]Gaussian units are the same as cgs emu for magnetostatics; Mx = maxwell, G = gauss, Oe = oersted; Wb = weber, V = volt, s = second, T = tesla, m = meter, A = ampere, J = joule, kg = kilogram, H = henry.

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Use either SI (MKS) or CGS as primary units. (SI units are strongly encouraged.) English units may be used as secondary units (in parentheses). **This applies to papers in data storage.** For example, write "15 Gb/cm^2 (100 Gb/in^2)." An exception is when English units are used as identifiers in trade, such as "3½-in disk drive." Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersteds. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity in an equation.

The SI unit for magnetic field strength H is A/m. However, if you wish to use units of T, either refer to magnetic flux density B or magnetic field strength symbolized as $\mu_0 H$. Use the center dot to separate compound units, e.g., "A·m^2."

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Multipliers can be especially confusing. Write "Magnetization (kA/m)" or "Magnetization (10^3 A/m)." Do not write "Magnetization (A/m) × 1000" because the reader would not know whether the top axis label in Fig. 1 meant 16000 A/m or 0.016 A/m. Figure labels should be legible, approximately 8 to 12 point type.

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Number citations consecutively in square brackets [1]. The sentence punctuation follows the brackets [2]. Multiple references [2], [3] are each numbered with separate brackets [1]–[3]. When citing a section in a book, please give the relevant page numbers [2]. In sentences, refer simply to the reference number, as in [3]. Do not use "Ref. [3]" or "reference [3]" except at the beginning of a sentence: "Reference [3] shows ... ." Please do not use automatic endnotes in *Word*, rather, type the reference list at the end of the paper using the "References" style.

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$$\int_0^{r_2} F(r,\varphi)\, dr\, d\varphi = [\sigma r_2 / (2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\, |z_j - z_i|)\, \lambda^{-1} J_1(\lambda r_2)\, J_0(\lambda r_i)\, d\lambda . \quad (1)$$

Be sure that the symbols in your equation have been defined before the equation appears or immediately following. Italicize symbols (*T* might refer to temperature,

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Use one space after periods and colons. Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." [It is not clear who or what used (1).] Write instead, "The potential was calculated by using (1)," or "Using (1), we calculated the potential."

Use a zero before decimal points: "0.25," not ".25." Use "cm^3," not "cc." Indicate sample dimensions as "0.1 cm × 0.2 cm," not "0.1 × 0.2 cm^2." The abbreviation for "seconds" is "s," not "sec." Do not mix complete spellings and abbreviations of units: use "Wb/m^2" or "webers per square meter," not "webers/m^2." When expressing a range of values, write "7 to 9" or "7-9," not "7~9."

A parenthetical statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.) In American English, periods and commas are within quotation marks, like "this period." Other punctuation is "outside"! Avoid contractions; for example, write "do not" instead of "don't." The serial comma is preferred: "A, B, and C" instead of "A, B and C."

If you wish, you may write in the first person singular or plural and use the active voice ("I observed that ..." or "We observed that ..." instead of "It was observed that ..."). Remember to check spelling. If your native language is not English, please get a native English-speaking colleague to carefully proofread your paper.

VI. Some Common Mistakes

The word "data" is plural, not singular. The subscript for the permeability of vacuum μ_0 is zero, not a lowercase letter "o." The term for residual magnetization is "remanence"; the adjective is "remanent"; do not write "remnance" or "remnant." Use the word "micrometer" instead of "micron." A graph within a graph is an "inset," not an "insert." The word "alternatively" is preferred to the word "alternately" (unless you really mean something that alternates). Use the word "whereas" instead of "while" (unless you are referring to simultaneous events). Do not use the word "essentially" to mean "approximately" or "effectively." Do not use the word "issue" as a euphemism for "problem." When compositions are not specified, separate chemical symbols by en-dashes; for example, "NiMn" indicates the intermetallic compound $Ni_{0.5}Mn_{0.5}$ whereas "Ni–Mn" indicates an alloy of some composition Ni_xMn_{1-x}.

Be aware of the different meanings of the homophones "affect" (usually a verb) and "effect" (usually a noun), "complement" and "compliment," "discreet" and "discrete," "principal" (e.g., "principal investigator") and "principle" (e.g., "principle of measurement"). Do not confuse "imply" and "infer."

Prefixes such as "non," "sub," "micro," "multi," and "ultra" are not independent words; they should be joined to the words they modify, usually without a hyphen. There is no period after the "et" in the Latin abbreviation "*et al.*" (it is also italicized). The abbreviation "i.e.," means "that is," and the abbreviation "e.g.," means "for example" (these abbreviations are not italicized).

An excellent style manual and source of information for science writers is [9]. A general IEEE style guide and an *Information for Authors* are both available at http://www.ieee.org/web/publications/authors/transjnl/index.html

VII. Editorial Policy

Submission of a manuscript is not required for participation in a conference. Do not submit a reworked version of a paper you have submitted or published elsewhere. Do not publish "preliminary" data or results. The submitting author is responsible for obtaining agreement of all coauthors and any consent required from sponsors before submitting a paper. IEEE Transactions and Journals strongly discourage courtesy authorship. It is the obligation of the authors to cite relevant prior work.

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1) Technical papers submitted for publication must advance the state of knowledge and must cite relevant prior work.
2) The length of a submitted paper should be commensurate with the importance, or appropriate to

the complexity, of the work. For example, an obvious extension of previously published work might not be appropriate for publication or might be adequately treated in just a few pages.

3) Authors must convince both peer reviewers and the editors of the scientific and technical merit of a paper; the standards of proof are higher when extraordinary or unexpected results are reported.
4) Because replication is required for scientific progress, papers submitted for publication must provide sufficient information to allow readers to perform similar experiments or calculations and use the reported results. Although not everything need be disclosed, a paper must contain new, useable, and fully described information. For example, a specimen's chemical composition need not be reported if the main purpose of a paper is to introduce a new measurement technique. Authors should expect to be challenged by reviewers if the results are not supported by adequate data and critical details.
5) Papers that describe ongoing work or announce the latest technical achievement, which are suitable for presentation at a professional conference, may not be appropriate for publication in a TRANSACTIONS or JOURNAL.

IX. CONCLUSION

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

APPENDIX

Appendixes, if needed, appear before the acknowledgment.

ACKNOWLEDGMENT

The preferred spelling of the word "acknowledgment" in American English is without an "e" after the "g." Use the singular heading even if you have many acknowledgments. Avoid expressions such as "One of us (S.B.A.) would like to thank ... ." Instead, write "F. A. Author thanks ... ." **Sponsor and financial support acknowledgments are placed in the unnumbered footnote on the first page, not here.**

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